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(54) Apparatus and method for encoding and reconstructing image data

Vorrichtung und Verfahren zur Kodierung und Wiederherstellung von Bilddaten

Appareil et procédé pour le codage et la reconstruction de données d'image

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Description

[0001] The present invention relates generally to a technique for both storing and outputting image data in a printing system and, more particularly, to an apparatus and method in which image data, from an input image, is encoded and the resulting encoded bitstream is then reconstructed.

[0002] Electronic printing systems typically include an input section, sometimes referred to as an input image terminal ("IIT"), a controller, sometimes referred to as an electronic subsystem ("ESS") and an output section or print engine, sometimes referred to as an image output terminal ("IOT"). In one type of electronic printing system, manufactured by Xerox® Corporation, known as the DocuTech® electronic printing system, a job can be inputted to the IIT from, among other sources, a network or a scanner. An example of an IIT with both network and scanner inputs is found in US-A-5,170,340.

[0003] It is known that output of an image can be enhanced significantly through use of a high addressability output device. For example, through employment of a printing machine with a capability of storing or buffering scanned data prepared at a resolution of 600 x 3 spi, a corresponding output of 1800 x 1 spi can be obtained. While this sort of output is desirable, storing image data at 600 x 3 spi, even for short time periods, can be burdensome on a printing machine with relatively limited volatile or system memory, such as some of the digital printing systems discussed above. While various ones of the above printing systems advantageously exploit disk storage, in conjunction with system memory, it is, for purposes of outputting a job, necessary to store or buffer the job in system memory. Moreover, even in a digital printing machine which takes advantage of disk, storage of an image is achieved, commonly, by "funneling" the image through the system memory on its way to disk. Such funneling process can "clog" up system memory readily when the image is relatively complex. It would be desirable to store or buffer a job in system memory of a high addressability printing machine, at a first resolution, and output it at a second resolution where the first resolution is significantly less than the second resolution.

[0004] In one example, storing or buffering a job at less than 600 x 3 spi is accomplished by discarding image-related information, i.e. image data. This discarding of image data can lead to a degradation of image quality when reproducing the remaining image data. It would be desirable to provide a technique in which at least a part of the discarded image data could be reconstructed so that image degradation is minimized.

[0005] It is an object of the present invention to provide a method and apparatus embodying such a technique.

[0006] This object is solved by a method according to claim 1 and an image processing apparatus according to claim 7.

[0007] Preferred embodiments are the subject-matters of the dependent claims.

[0008] The invention will become apparent from the following description, the description being used to illustrate a preferred embodiment of the invention when read in conjunction with the accompanying drawings, in which:-

Figure 1 is a block diagram depicting a multifunctional, network adaptive printing machine;
Figure 2 is a block diagram of a video control module for the printing machine of Figure 1;
Figure 3 is a block diagram of a transfer module used in conjunction with the printing machine of Figure 2;
Figure 4 is a block diagram of a facsimile card used in conjunction with the printing machine of Figure 2;
Figure 5 is a block diagram of a network controller for the printing machine of Figure 1;
Figures 6 and 7 represent a flow diagram depicting a technique for encoding and reconstructing an input image;
Figure 8 is a schematic representation depicting an encoding scheme of the present technique;
Figure 9 is a schematic representation of an analyzing circuit used in a reconstruction arrangement of the present technique;
Figure 10 is a schematic representation of the contents of a look-up table of Figure 9;
Figures 11A and 11B are schematic, partial representations of scanlines, the schematic, partial representations being employed to illustrate one aspect of the present technique;
Figure 12 is a schematic representation of another analyzing circuit used in conjunction with one aspect of the present technique;
Figure 13 is a schematic representation of a multiplexing arrangement used in conjunction with the analyzing circuit of Figure 12;
Figure 14 is a schematic representation of a select circuit used to generate the select signals for the multiplexing arrangement of Figure 13;
Figure 15 is schematic representation of another multiplexing arrangement usable with the analyzing circuit of Figure 12; and
Figure 16 is a schematic representation of a printer with a pulse width position modulator, the pulse width position modulator being responsive to encoded/reconstructed data generated in accordance with the present technique.

[0009] Referring to Figure 1, a multifunctional, network adaptive printing system is designated by the numeral 10. The printing system 10 includes a printing machine 12 operatively coupled with a network service module 14. The printing machine 12 includes an electronic subsystem 16, referred to as a video control module (VCM), communicating with a scanner 18 and a

printer 20. In one example, the VCM 16, which will be described in further detail below, coordinates the operation of the scanner and printer in a digital copying arrangement. In a digital copying arrangement, the scanner 18 (also referred to as image input terminal (IIT)) reads an image on an original document by using a CCD full width array and converts analog video signals, as gathered, into digital signals. In turn, an image processing system 22 (Figure 2), associated with the scanner 18, executes signal correction and the like, converts the corrected signals into multi-level signals (e.g. binary signals), compresses the multi-level signals and preferably stores the same in electronic precollation (EPC) memory 24.

[0010] Referring again to Figure 1, the printer 20 (also referred to as image output terminal (IOT)) preferably includes a xerographic print engine. In one example, the print engine has a multi-pitch belt (not shown) which is written on with an imaging source, such as a synchronous source (e.g. laser raster output scanning device) or an asynchronous source (e.g. LED print bar). In a printing context, the multi-level image data is read out of the EPC memory 24 (Figure 2) while the imaging source is turned on and off, in accordance with the image data, forming a latent image on the photoreceptor. In turn, the latent image is developed with, for example, a hybrid jumping development technique and transferred to a print media sheet. Upon fusing the resulting print, it may be inverted for duplexing or simply outputted. It will be appreciated by those skilled in the art that the printer can assume other forms besides a xerographic print engine without altering the concept upon which the disclosed embodiment is based. For example, the printing system 10 could be implemented with a thermal ink jet or ionographic printer.

[0011] Referring specifically to Figure 2, the VCM 16 is discussed in further detail. The VCM 16 includes a video bus (VBus) 28 with which various I/O, data transfer and storage components communicate. Preferably, the VBus is a high speed, 32 bit data burst transfer bus which is expandable to 64 bit. The 32 bit implementation has a sustainable maximum bandwidth of approximately 60 MBytes/sec. In one example, the bandwidth of the VBus is as high as 100 MBytes/sec.

[0012] The storage components of the VCM reside in the EPC memory section 30 and the mass memory section 32. The EPC memory section includes the EPC memory 24, the EPC memory being coupled with the VBus by way of a DRAM controller 33. The EPC memory, which is preferably DRAM, provides expansion of up to 64 MBytes, by way of two high density 32 bit SIMM modules. The mass memory section 32 includes a SCSI hard drive device 34 coupled to the VBus by way of a transfer module 36a. As will appear, other I/O and processing components are coupled respectively to the VBus by way of transfer modules 36. It will be appreciated that other devices (e.g. a workstation) could be coupled to the VBus by way of the transfer module 36a through use of a suitable interface and a SCSI line.

[0013] Referring to Figure 3, the structure of one of the transfer modules 36 is discussed in further detail. The illustrated transfer module of Figure 3 includes a packet buffer 38, a VBus interface 40 and DMA transfer unit 42 . The transfer module 36, which was designed with "VHSIC" Hardware Description Language (VHDL), is a programmable arrangement permitting packets of image data to be transmitted along the VBus at a relatively high transfer rate. In particular, the packet buffer is programmable so that the segment or packet can be varied according to the available bandwidth of the VBus. In one example, the packet buffer can be programmed to handle packets of up to 64 Bytes Preferably, the packet size would be reduced for times when the VBus is relatively busy and increased for times when activity on the bus is relatively low.

[0014] Adjustment of the packet size is achieved with the VBus interface 40 and a system controller 44 (Figure 5). Essentially, the VBus interface is an arrangement of logical components, including, among others, address counters, decoders and state machines, which provides the transfer module with a selected degree of intelligence. The interface 40 communicates with the system controller to keep track of desired packet size and, in turn, this knowledge is used to adjust the packet size of the packet buffer 38, in accordance with bus conditions. That is, the controller, in view of its knowledge regarding conditions on the VBus 28, passes directives to the interface 40 so that the interface can adjust packet size accordingly. Further discussion regarding operation of the transfer module 36 is provided below

[0015] More particularly, each DMA transfer unit employs a conventional DMA transfer strategy to transfer the packets. In other words, the beginning and end addresses of the packet are used by the transfer unit in implementing a given transfer. When a transfer is complete, the interface 40 transmits a signal back to the system controller 44 so that further information, such as desired packet size and address designations, can be obtained.

[0016] Referring to Figures 1 and 2, three I/O components are shown as being coupled operatively to the VBus 28, namely a FAX module 48, the scanner or IIT 18, and the printer or IOT 20; however, it should be recognized that a wide variety of components could be coupled to the VBus by way an expansion slot 50. Referring to Figure 4, an implementation for the FAX module, which is coupled to the VBus 28 by way of transfer module 36b, is discussed in further detail. In the preferred embodiment, a facsimile device (FAX) 51 includes a chain of components, namely a section 52 for performing Xerox adaptive compression/decompression, a section 54 for scaling compressed image data, a section 56 for converting compressed image data to or from CCITT format, and a modem 58, preferably manufactured by Rockwell Corporation, for transmitting CCITT formatted data from or to a telephone, by way of a conventional

communication line.

[0017] Referring still to Figure 4, each of the sections 52, 54 and 56 as well as modem 58 are coupled with the transfer module 36b by way of a control line 60. This permits transfers to be made to and from the FAX module 48 without involving a processor. As should be understood, the transfer module 36b can serve as a master or slave for the FAX module in that the transfer module can provide image data to the FAX for purposes of transmission or receive an incoming FAX. In operation, the transfer module 36b reacts to the FAX module in the same manner that it would react to any other I/O component. For example, to transmit a FAX job, the transfer module 36b feeds packets to the section 52 through use of the DMA transfer unit 42 and, once a packet is fed, the transfer module transmits an interrupt signal to the system processor 44 requesting another packet. In one embodiment, two packets are maintained in the packet buffer 38 so that "ping-ponging" can occur between the two packets. In this way, the transfer module 36b does not run out of image data even when the controller cannot get back to it immediately upon receiving an interrupt signal.

[0018] Referring again to Figure 2, the IIT 18 and IOT 20 are operatively coupled to the VBus 28 by way of transfer modules 36c and 36d. Additionally, the IIT 18 and the IOT 20 are operatively coupled with a compressor 62 and a decompressor 64, respectively. The compressor and decompressor are preferably provided by way of a single module that employs Xerox adaptive compression devices. Xerox adaptive compression devices have been used for compression/decompression operations by Xerox Corporation in its DocuTech® printing system. In practice, at least some of the functionality of the transfer modules is provided by way of a 3 channel DVMA device, which device provides local arbitration for the compression/decompression module.

[0019] As further illustrated by Figure 2, the scanner 18, which includes the image processing section 22, is coupled with an annotate/merge module 66. Preferably the image processing section includes one or more dedicated processors programmed to perform various desired functions, such as image enhancement, thresholding/screening, rotation, resolution conversion and TRC adjustment. The selective activation of each of these functions can be coordinated by a group of image processing control registers, the registers being programmed by the system controller 44. Preferably, the functions are arranged along a "pipeline" in which image data is inputted to one end of the pipe, and image processed image data is outputted at the other end of the pipe. To facilitate throughput, transfer module 36e is positioned at one end of the image processing section 22 and transfer module 36c is positioned at another end of the section 22. As will appear, positioning of transfer modules 36c and 36e in this manner greatly facilitates the concurrency of a loopback process.

[0020] Referring still to Figure 2, arbitration of the various bus masters of the VCM 16 is implemented by way of a VBus arbiter 70 disposed in a VBus arbiter/bus gateway 71. The arbiter determines which bus master (e.g. FAX module, Scanner, Printer, SCSI Hard Drive, EPC Memory or Network Service Component) can access the VBus at one given time. The arbiter is made up of two main sections and a third control section. The first section, i.e., the "Hi-Pass" section, receives input bus requests and current priority selection, and outputs a grant corresponding to the highest priority request pending. The current priority selection input is the output from the second section of the arbiter and is referred to as "Priority Select". This section implements priority rotation and selection algorithm. At any given moment, the output of the logic for priority select determines the order in which pending requests will be serviced. The input to Priority Select is a register which holds an initial placement of devices on a priority chain. On servicing requests, this logic moves the devices up and down the priority chain thereby selecting the position of a device's next request. Control logic synchronizes the tasks of the Hi-Pass and the Priority Select by monitoring signals regarding request/grant activity. It also prevents the possibility of race conditions.

[0021] Referring to Figure 5, the network service module 14 is discussed in further detail. As will be recognized by those skilled in the art, the architecture of the network service module is similar to that of a known "PC clone". More particularly, in the preferred embodiment, the controller 44, which preferably assumes the form of a SPARC processor, manufactured by Sun Microsystems, Inc., is coupled with a standard SBus 72. In the illustrated embodiment of Figure 5, a host memory 74, which preferably assumes the form of DRAM, and a SCSI disk drive device 76 are coupled operatively to the SBus 72. While not shown in Figure 5, a storage or I/O device could be coupled with the SBus with a suitable interface chip. As further shown in Figure 5, the SBus is coupled with a network 78 by way of an appropriate network interface 80. In one example, the network interface includes all of the hardware and software necessary to relate the hardware/software components of the controller 44 with the hardware/software components of the network 78. For instance, to interface various protocols between the network service module 14 and the network 78, the network interface could be provided with, among other software, Netware® from Novell Corp.

[0022] In one example, the network 78 includes a client, such as a workstation 82 with an emitter or driver 84. In operation, a user may generate a job including a plurality of electronic pages and a set of processing instructions. In turn, the job is converted, with the emitter, into a representation written in a page description language, such as PostScript. The job is then transmitted to the controller 44 where it is interpreted with a decomposer, such as one provided by Adobe Corporation.

[0023] Referring again to Figure 2, the network service module 14 is coupled with the VCM 16 via a bus gate-

way 88 of the VBus arbiter/bus gateway 71. In one example, the bus gateway comprises a field programmable gate array provided by XILINX corporation. The bus gateway device provides the interface between the host SBus and the VCM VBus. It provides VBus address translation for accesses to address spaces in the VBus real address range, and passes a virtual address to the host SBus for virtual addresses in the host address range. A DMA channel for memory to memory transfers is also implemented in the bus gateway. Among other things, the bus gateway provides seamless access between the VBus and SBus, and decodes virtual addresses from bus masters, such as one of the transfer modules 36, so that an identifier can be obtained from a corresponding slave component. It will be appreciated by those skilled in the art that many components of the printing system 10 are implemented in the form of a single ASIC.

[0024] Referring to Figures 2, 3 and 5, further discussion regarding DMA transfer of each of the transfer modules 36 is provided. In particular, in one example, the images of a job are stored in the host memory 74 as a series of blocks which are stored in the EPC memory 24. Preferably, each block comprises a plurality of packets. In operation, one of the transfer modules 36 is provided, by the controller 44, with the beginning address of a block and the size of the block. In turn, for that block, the transfer module 36 effects a packet tranfer and increments/decrements a counter. This procedure is repeated for each packet of the block until the interface 40 determines, by reference to the counter, that the last packet of the block has been transferred. Typically, for each stored image, several blocks are transferred, in a packet-by-packet manner, as described immediately above.

[0025] Referring to Figures 2, 5, 6 and 7, an image processing technique, appropriate for use with printing system 10, is discussed. In the illustrated embodiment of Figure 6, input image data, for a given input image, is, at step 400, inputted to image processing section 22 (Figure 2). In one mode of operation, the inputted image data is obtained at the scanner 18. More particularly, a document is scanned and 2^x bits of gray data is provided in the form of a bitstream. In turn, the gray data is thresholded so that the image is expressed as n bits of data where n is less than 2^x. In one example, the given input image is processed at 600 x 3 spi so that n = 3 and a resulting output, with a resolution of 1800 x 1 spi, can be obtained. It has been found, however, as explained in further detail below, that, for this example, storage can be optimized and an output resolution of 1800 x 1 spi obtained even when the value of n is less than 3. As will appear, the present technique is applicable for inputs and outputs of various resolutions, and image data can be obtained from a wide range of input sources without affecting the concept underlying the disclosed embodiment.

[0026] In accordance with the preferred technique, at step 402, image data is encoded. Referring to the illustrated embodiment of Figure 8, n bits are described with n - m bits where each m bit represents, as explained in further detail below, positional information. In one example, three bits are described generally with two bits, or, stated alternatively, at one of four levels. It follows from the illustration of Figure 8, that in a high addressability approach, each 600 x 2 pixel can be encoded so as to simulate 1800 x 1 data. Normally, three bits would be required to describe three pixels at 1800 x 1 spi, but in the illustrated scheme of Figure 8, only two bits, designated by the term "intensity", are required to describe a group of three 1800 x 1 spi pixels. That is a 600 x 2 spi pixel, with an intensity of 00, is equivalent to three white pixels at 1800 x 1 output, a 600 x 2 spi pixel, with an intensity of 01, is equivalent to one black pixel and two white pixels, at 1800 x 1 spi, and so on.

[0027] It should be recognized, nonetheless that certain image-related information is lost by the encoding scheme of Figure 8 in that the pixels labeled as "GRAY1" and "GRAY2" cannot be fully described by just two bits. In other words, use of only two bits does not indicate whether the black pixel is left justified, right justified or center justified. Effectively, as explained in further detail below, this information can be provided, via a reconstruction step.

[0028] Referring again to Figures 2 and 6, preferably, an encoded bitstream is compressed, with compressor 62 (step 404) and then stored in EPC memory 24 (step 406). The compressed, encoded bitstream is, via step 408, held in the EPC memory until it is either copied to disk 34 (step not shown) or outputted to an appropriate output device, such as the printer 20. When it is time to output the stored encoded bitstream, decompression is effected, via step 410, with the decompressor 64. As will be appreciated from the discussion above, movement of data between the image processing section, compressor, EPC memory and the decompressor, is facilitated with the transfer modules 36.

[0029] In anticipation of outputting the image data, the corresponding bitstream is analyzed, per step 412, with a bitstream analyzing arrangement. Referring generally to Figures 9-13, an example of a reconstruction scheme, with a bitstream analyzer is illustrated. It will be appreciated by those skilled in the art that operation of the bitstream analyzer can be implemented with a suitable processor. Moreover, the image assumes the form of a bitmap with a plurality of scanlines.

[0030] Referring to Figures 6, 8 and 9, when a present or central pixel 411a corresponds with three white or three black pixels, then the central pixel can be described completely with two bits. In the case of an all white or all black central pixel 411a, the process proceeds to step 452 (Figure 7). When, however, the central pixel is GRAY1 (i.e. "G1") or GRAY2 (i.e. "G2") pixel (step 413), then the central pixel cannot be described with two bits.

[0031] Referring specifically to Figure 9, a preferred

approach for interpreting G1 and G2 central pixels is discussed. In the preferred approach, each pixel for a given input bitstream is read for purposes of comparing bit pairs representative of "neighboring" or "framing" pixels with the entries of a 16 x 1 look-up table. More particularly, each central pixel 411a is disposed intermediate of a left neighbor pixel 411b and a right neighbor pixel 411c. In one example of operation, the respective bit pairs of the left neighbor and the right neighbor, for each G or G2 pixel, are compared to each of sixteen bit pairs in the look-up table 415 of Figure 10. In turn, a match is obtained and a corresponding positional signal or value is assigned to the central or present pixel.

[0032] The positional signal of the illustrated look-up table facilitates a reconstruction of the bit discarded during the encoding of the image data. More particularly, it is known that, in a typical black and white image, black pixels tend to group together. Accordingly, this knowledge can be used in reconstructing the present pixel of Figure 8 when that pixel assumes the form of the G1 pixel or the G2 pixel. It stands to reason that the gray part of a G1 or G2 central pixel would tend to associate with the neighboring pixel having the greatest intensity.

[0033] This approach can be best understood by reference to an example of Figures 11A and 11B. The pixel 411b, which has an intensity of 11, is referred to, in the look-up table 415 (Figure 10), as "B" and the pixel 411c, which has an intensity of 00, is referred to, in the look-up table, as "W". As indicated by the look-up table, the position of the gray pixel in the present pixel is left justified (Figure 8) so that the one black pixel of the pixel 411a is grouped with the black pixels 411b-1, 411b-2 and 411b-3 of pixel 411b. It will be appreciated that while the current methodology groups black pixels, in another approach, white pixels could be grouped together.

[0034] The approach discussed above assumes that the left neighbor pixel and the right neighbor pixel have different intensities. When this assumption holds true, the process proceeds to step 422 (Figure 6), and then step 424 where a positional signal of "0" or "1" is assigned to the central or present pixel 411A. It should be appreciated that a single bit cannot designate each case for a GRAY1 pixel in that an 1800 x 1 pixel (Figure 8) can assume one of three positions. The present technique assumes that the 1800 x 1 pixel is either left or right justified. In another embodiment, center justification would be accommodated for by using two bits to describe the positional signal. It will be recognized that use of two bits to describe justification provides additional flexibility to the current technique.

[0035] Referring to Figure 10, for the case in which the left neighbor pixel/right neighbor pixel pair is W-W, an ambiguity exists because there is no reason, based on a single scanline analysis, for justifying the gray part of the present pixel to the left or to the right. In the illustrated embodiment of Figure 10, the positional signal or value of the the four cases is assigned on the basis of empirical observations regarding image data output.

Referring generally to Figures 12-14, an approach for optimizing the present technique, when the left neighbor pixel/right neighbor pixel pair is W-W, is discussed.

[0036] Referring conjunctively to Figures 6 and 12, when the present or central pixel 411a of a scanline 411 being processed cannot be assigned a positional signal, because the respective intensities of the left neighbor pixel and the right neighbor pixel are white (step 426), a corresponding two pixels of a previous scanline 428 are examined (step 430) with the bitstream analyzer. To effect the examination, a second 16 x 1 look-up table 432, identical to the one of Figures 10 and 12, namely look-up table 415, is employed. If a match is found in the second look-up table, and the match does not relate to a bit pair in which the intensities are the same (e.g. the intensities are W-W), then a positional signal is obtained in the same manner as described for step 424.

[0037] Referring to Figures 17 and 12, if the positional signal for the present pixel cannot be designated, by reference to the previous scanline, because the respective intensities of the corresponding pixels of the previous scanline are, for example, both white, then, via step 436, the intensities of a corresponding two pixels of a next scanline 438 are examined with a third look-up table 440, which third look-up table is identical in content to the first look-up table 434. If a match is found in the third look-up table, and the match does not relate to a bit pair in which the intensities are each white, then a positional signal is obtained in the same manner as described for step 424. If a match cannot be made on the basis of examining any of the scanlines 425, 428 or 438, then, via steps 444, 446, default positional value is, via step 446, assigned.

[0038] In the illustrated embodiment of Figures 6, 7 and 12, the three scanlines are analyzed simultaneously to determine what the positional signal of the present pixel should be Preferably, one of a plurality of output signals from the look-up tables 415, 432 and 440 is then chosen with a 4 to 1 multiplexer 450 (Figure 13), which multiplexer is controlled by selected signals designated as "SEL0" and SEL1". Referring to Figure 14, an implementation for generating the select signals is shown. Referring conjunctively to Figures 13 and 14, when the respective signals of SEL0 and SEL1 are 1 and 1, the positional signal of look-up table 415 is permitted to pass through a multiplexer 450. When the respective signals of SEL0 and SEL1 are 1 and 0, the positional signal of look-up table 432 is permitted to pass through the multiplexer 450. When the respective signals of SEL0 and SEL1 are 0 and 1, the positional signal of look-up table 440 is permitted to pass through the multiplexer 450. In a default case, namely when the respective signals of SEL0 and SEL1 are 0 and 0, a preassigned signal, e.g. a 1, is permitted to pass through the multiplexer 450. It will be appreciated that the preassigned signal may be assigned, for example, on the basis of empirical data.

[0039] Referring to Figure 15, in another embodiment, the position signal for the present pixel 423 could be ob-

tained through the use of an arrangement with just one of the look-up tables 416, 434 or 440 and the multiplexer 450. More particularly, in this other embodiment, the bits corresponding to each of the framing or neighboring pixels of scanlines 411, 428 and 438, along with a suitable set of default bits, is transmitted to the four inputs of the multiplexer 450. Through use of appropriate select signals, from the select circuit of Figure 14, one of the bit sets is permitted to pass through the multiplexer, and, in turn, that bit set is processed with the look-up table.

[0040] Referring again to Figure 7, subsequent to the assignment of each positional signal, a check is performed, at step 352, to determine if all of the image data for a given input image has been processed. If an end to the image data has not been reached, then the neighboring pixels of another central pixel are examined (step 454) and the process returns to step 424. If, on the other hand, all of the image data for the given input image has been processed, then the image data of the given input image is prepared for output.

[0041] Referring to Figure 16, in one example of output, namely marking, the image data is transmitted to the printer 20, the printer 20 including a component 456 referred to as a pulse width position modulator ("PWPM"). As is known, the PWPM serves to control the operation of a raster output scanner ("ROS") as a function of digital input provided thereto. In the illustrated embodiment of Figure 16, the PWPM is responsive to the representative bits of a given pixel and, where appropriate, a positional signal so that three output pixels are reproduced by the ROS on the basis of the two or three bits provided to the PWPM. In one example, as shown in Figure 16, when the input data is a 01 and the positional signal is 1, the output includes two white pixels and one black pixel with the black pixel being left justified.

[0042] Numerous features of the above-disclosed embodiment will be appreciated by those skilled in the art:

[0043] First, the present technique includes an encoding approach which permits m out of every n bits to be discarded from image data of an input image where the m bits represent "positional" bits and n - m bits correspond with 2^{n-m} intensities. This discarding of bits results in a decrease of storage demand. In one example a storage saving of up to 33% is achieved. In some cases, such as the ones in which a pixel is all white or all black, the discarded bit will not be missed. That is, in some instances, it is possible to describe, completely, the output states of n bits with just n - m bits. In any event, "lost" information provided by the discarded bits is, where necessary, reconstructed, so there is little or no loss in image output quality.

[0044] Reconstruction is preferably accomplished by examining each pixel in an image and assigning a positional signal, when appropriate. Such reconstruction is believed to be necessary when the position of one or two black pixels, disposed in a group of three pixels cannot be positioned or justified on the basis of two bits worth of image information. Due to the assignment of the positional signals, virtually all of the information, related to the input image, can be recaptured for output.

[0045] Second, each positional signal is assigned with a high degree of accuracy. In one example, when a pixel being examined is framed by two pixels of the same intensity, e.g. white pixels, corresponding pixels from adjacent scanlines are analyzed to optimize eventual justification of one or more black pixels. Additionally, the examined pixels of the multiple scanlines can be analyzed in parallel so that the best suited positional signal can be obtained within a relatively short time interval.

[0046] Finally, relatively little hardware and software are required to implement the present technique. More particularly, each time a bit is discarded, an efficient encoding scheme is employed to compensate for much of the apparent loss in information. Moreover, pursuant to output of the encoded data, use of a simple, yet intuitive algorithm provides for the assignment of the positional signals. This algorithm is implemented with a minimum amount of hardware and, in one example, a suitable implementation can be achieved with relatively few logical components and a single look-up table.

Claims

1. A method of processing an input image with a printing system (10) having an electronic volatile memory (74), said input image being represented by image data, in the form of a data stream, comprising a plurality of successive bits grouped into first bit sets (411A, 411B, 411C)
each set comprising n bits, comprising the steps of:

encoding (402) said first bit sets into second bit sets (00, 01, 10, 11), each of the second bit sets having less bits (n-m) than each of the first bit sets, m being the number of discarded bits in each bit set as a result of said encoding;

storing (406) the encoded bit stream in the electronic volatile memory (74) with memory space being saved as a result of reducing a size of each of the first bit sets;

analyzing the stored encoded bit stream by defining a center second bit set disposed between a left second bit set and a right second bit set, respectively, for generating a corresponding signal assigned to said center second bit set and determined by comparing the intensities of said left second bit set and said right second bit set;

reconstructing the stored encoded bit stream, by converting the second bit sets to third bit

sets, each of said third bit sets again having n bits, the bits of said center bit set being arranged on the basis of said signal such that the bits representing black colour of said center bit set are associated to that one of said left or right neighbouring bit sets possessing the greater intensity; and

outputting an image representation of the reconstructed bit stream.

2. The method of claim 1, in which each first and second bit set corresponds with a pixel and the pixels are disposed in a plurality of scanlines, wherein said analyzing step is performed on each scanline.

3. The method of claim 2, further comprising the step of providing a look-up table (415), in a second electronic memory (434), the look-up table including a plurality of intensity pairs, each pair being mapped to one of said signals, respectively, and wherein: said analyzing step includes matching the respective intensities of the pixels left and right to a center pixel with one of the intensity pairs in the look-up table to obtain said corresponding signal.

4. The method of claim 3, in which, where the intensity of the left pixel is the same as that one of the right pixel, said analyzing step analyzes:

at least one neighbouring scanline (428) with a fourth pixel disposed between a fifth pixel and a sixth pixel at a position corresponding to the position of said center, left and right pixels respectively and examining the respective intensities of the fifth and sixth pixels; and

determining said signal of the center pixel in accordance with the signals obtained by analyzing the at least one neighbouring scanline.

5. The method of one of claims 1 to 4, wherein said outputting step comprises printing the image, on a substrate, with a print engine (20).

6. The method of one of claims 1 to 5, wherein said encoding step includes encoding the bit stream with an image processing device (22).

7. An apparatus for processing an input image represented by image data in the form of a data stream comprising a plurality of successive bits grouped into first bit sets (411A, 411B, 411C), each bit set comprising n bits, comprising:

a device for encoding (62) said first bit sets into second bit sets (00, 01, 10, 11), each of the second bit sets having less bits (n-m) than each of the first bit sets, m being the number of discarded bits in each bit set as a result of said encoding;

an electronic volatile memory (74) for storing (406) the encoded bit stream in the electronic volatile memory (74) with memory space being saved as a result of reducing a size of each of the first bit sets;

a bit stream analyzer (415, 432, 440; 434) for analyzing the stored encoded bit stream by defining a center second bit set disposed between a left second bit set and a right second bit set, respectively for generating a corresponding signal assigned to said center second bit set and determined by comparing the intensities of said left second bit set and said right second bit set;

a reconstruction circuit (64; 20) for reconstructing the stored encoded bit stream by converting the second bit sets to third bit sets, each of said third bit sets again having n bits, the bits of said center bit set being arranged on the basis of said signal, such that the bits representing black color of said center bit set are associated to that one of said left or right neighbouring bit sets possessing the greater intensity; and

an output device (20; 51, 28) for outputting an image representation of the reconstructed bit stream.

8. The image processing apparatus of claim 7, in which each first and second bit set corresponds with a pixel and the pixels are disposed in a plurality of scanlines (411, 428, 438).

9. The image processing apparatus of claim 8, in which said bitstream analyzer (415, 440; 434) includes a look-up table (LUT; 415), in a second electronic memory (432), the look-up table including a plurality of intensity pairs, each pair being mapped to one of said signals, respectively, and wherein the respective intensities of the pixels left and right to a center pixel are matched in the bitstream analyzer with one of the intensity pairs in the look-up table to obtain the corresponding signal.

10. The image processing apparatus of claim 9, in which, where the intensity of the left pixel is the same as that one of the right pixel, said bitstream analyzer analyzes at least one neighbouring scanline (428) with a fourth pixel disposed between a fifth pixel and a sixth pixel at a position corresponding to the position of said center, left and right pixels respectively; examines the respective intensities of

the fifth and sixth pixels, and determines said signal of the center pixel in accordance with the signals obtained by analyzing said at least one neighbouring scanline.

Patentansprüche

1. Verfahren zum Verarbeiten eines Eingangs-Bilds mit einem Drucksystem (10), das einen elektronischen, flüchtigen Speicher (74) besitzt, wobei das Eingangs-Bild durch Bild-Daten, in der Form einer Datenfolge, dargestellt ist, aufweisend eine Vielzahl von aufeinanderfolgenden Bits, die in erste Bit-Sätze (411A, 411B, 411C) gruppiert sind, wobei jeder Satz n Bits aufweist, mit den Schritten:

   Codieren (402) der ersten Bit-Sätze in zweite Bit-Sätze (00, 01, 10, 11), wobei jeder der zweiten Bit-Sätze weniger Bits (n-m) als jeder der ersten Bit-Sätze besitzt, wobei m die Zahl von ausgesonderten Bits in jedem Bit-Satz als eine Folge des Codierens ist;
   Speichern (406) der codierten Bit-Folge in dem elektronischen, flüchtigen Speicher (74), wobei Speicherraum als Folge eines Reduzierens einer Größe jedes der ersten Bit-Sätze eingespart wird;
   Analysieren der gespeicherten, codierten Bit-Folge durch Definieren eines zentralen, zweiten Bit-Satzes, angeordnet zwischen einem linken, zweiten Bit-Satz und einem rechten, zweiten Bit-Satz jeweils, zum Erzeugen eines entsprechenden Signals, das zu dem mittleren, zweiten Bit-Satz zugeordnet ist und durch Vergleichen der Intensitäten des linken, zweiten Bit-Satzes und des rechten, zweiten Bit-Satzes bestimmt ist;
   Rekonstruieren der gespeicherten, codierten Bit-Folge durch Wandeln der zweiten Bit-Sätze zu dritten Bit-Sätzen, wobei jeder der dritten Bit-Sätze wiederum n Bits besitzt, wobei die Bits des mittleren Bit-Satzes auf der Basis des Signals so angeordnet werden, daß die Bits, die eine schwarze Farbe des mittleren Bit-Satzes darstellen, zu dem einen des linken oder rechten, benachbarten Bit-Satzes zugeordnet werden, der die größere Intensität besitzt; und
   Ausgeben einer Bild-Darstellung der rekonstruierten Bit-Folge.

2. Verfahren nach Anspruch 1, wobei jeder erste und zweite Bit-Satz einem Pixel entspricht und die Pixel in einer Mehrzahl von Abtastlinien angeordnet sind, wobei der analysierende Schritt in Bezug auf jede Abtastlinie durchgeführt wird.

3. Verfahren nach Anspruch 2, das weiterhin den Schritt eines Vorsehens einer Durchsichtstabelle (415), in einem zweiten, elektronischen Speicher (434), aufweist, wobei die Durchsichtstabelle eine Vielzahl von Intensitäts-Paaren umfaßt, wobei jedes Paar zu einem der Signale jeweils aufgelistet wird, und wobei:

   der analysierende Schritt ein Anpassen der jeweiligen Intensitäten der Pixel links und rechts zu einem mittleren Pixel mit einem der Intensitäts-Paare in der Durchsichtstabelle, um das entsprechende Signal zu erhalten, umfaßt.

4. Verfahren nach Anspruch 3, wobei dort, wo die Intensität des linken Pixels dieselbe wie die eine des rechten Pixels ist, der analysierende Schritt analysiert:

   mindestens eine benachbarte Abtastlinie (428) mit einem vierten Pixel, angeordnet zwischen einem fünften Pixel und einem sechsten Pixel an einer Position entsprechend zu der Position des mittleren, linken und rechten Pixels jeweils, und wobei die jeweiligen Intensitäten des fünften und sechsten Pixels geprüft werden; und wobei das Signal des mittleren Pixels entsprechend den Signalen, die durch Analysieren der mindestens einen benachbarten Abtastlinie erhalten sind, bestimmt wird.

5. Verfahren nach einem der Ansprüche 1 bis 4, wobei der Ausgabe-Schritt ein Drukken des Bilds, auf einem Substrat, mit einer Druckmaschine (20) aufweist.

6. Verfahren nach einem der Ansprüche 1 bis 5, wobei der Codier-Schritt ein Codieren der Bit-Folge mit einer Bildverarbeitungs-Vorrichtung (22) umfaßt.

7. Vorrichtung zum Verarbeiten eines Eingangs-Bilds, das durch Bild-Daten, in der Form einer Datenfolge, dargestellt ist, die eine Vielzahl von aufeinanderfolgenden Bits aufweist, die in erste Bit-Sätze (411A, 411B, 411C) gruppiert sind, wobei jeder Bit-Satz n Bits aufweist, mit:

   einer Vorrichtung zum Codieren (62) der ersten Bit-Sätze in zweite Bit-Sätze (00, 01, 10, 11), wobei jeder der zweiten Bit-Sätze weniger Bits (n-m) als jeder der ersten Bit-Sätze besitzt, wobei m die Zahl von ausgesonderten Bits in jedem Bit-Satz als Folge des Codierens ist;
   einem elektronischen, flüchtigen Speicher (74) zum Speichern (406) der codierten Bit-Folge in dem elektronischen, flüchtigen Speicher (74), wobei Speicherraum als eine Folge eines Reduzierens einer Größe jeder der ersten Bit-Sätze eingespart wird;

einem Bit-Folge-Analysierer (415, 432, 440; 434) zum Analysieren der gespeicherten, codierten Bit-Folge durch Definieren eines mittleren, zweiten Bit-Satzes, angeordnet zwischen einem linken, zweiten Bit-Satz und einem rechten, zweiten Bit-Satz jeweils, zum Erzeugen eines entsprechenden Signals, das dem mittleren, zweiten Bit-Satz zugeordnet ist und durch Vergleichen der Intensitäten des linken, zweiten Bit-Satzes und des rechten, zweiten Bit-Satzes, bestimmt ist;
einer Rekonstruktions-Schaltung (64; 20) zum Rekonstruieren der gespeicherten, codierten Bit-Folge durch Wandeln der zweiten Bit-Sätze in dritte Bit-Sätze, wobei jeder der dritten Bit-Sätze wiederum n Bits besitzt, wobei die Bits des mittleren Bit-Satzes auf der Basis des Signals angeordnet werden, so daß die Bits, die eine schwarze Farbe des mittleren Bit-Satzes darstellen, zu demjenigen einen des linken oder rechten, benachbarten Bit-Satzes, der die größere Intensität besitzt, zugeordnet sind; und einer Ausgabe-Vorrichtung (20; 51, 28) zum Ausgeben einer Bild-Darstellung der rekonstruierten Bit-Folge.

8. Bildverarbeitungs-Vorrichtung nach Anspruch 7, wobei jeder erste und zweite Bit-Satz einem Pixel entspricht und die Pixel in einer Vielzahl von Abtastlinien (411, 428, 438) angeordnet sind.

9. Bildverarbeitungs-Vorrichtung nach Anspruch 8, wobei der Bit-Folge-Analysierer (415, 440; 434) eine Durchsichtstabelle (LUT; 415), in einem zweiten, elektronischen Speicher (432), umfaßt, wobei die Durchsichtstabelle eine Vielzahl von Intensitäts-Paaren umfaßt, wobei jedes Paar zu einem der Signale jeweils aufgelistet ist, und wobei die jeweiligen Intensitäten der Pixel links und rechts zu einem mittleren Pixel in dem Bit-Folge-Analysierer zu einem der Intensitäts-Paare in der Durchsichtstabelle angepaßt sind, um das entsprechende Signal zu erhalten.

10. Bildverarbeitungs-Vorrichtung nach Anspruch 9, wobei dort, wo die Intensität des linken Pixels dieselbe wie diejenige eine des rechten Pixels ist, der Bit-Folge-Analysierer mindestens eine benachbarte Abtastlinie (428) analysiert, mit einem vierten Pixel, das zwischen einem fünften Pixel und einem sechsten Pixel an einer Position entsprechend zu der Position des mittleren, linken und rechten Pixels jeweils angeordnet ist; die jeweiligen Intensitäten des fünften und sechsten Pixels prüft und das Signal des mittleren Pixels entsprechend den Signalen, die durch Analysieren der mindestens einen benachbarten Abtastlinie erhalten sind, bestimmt.

Revendications

1. Procédé de traitement d'une image d'entrée avec un système d'impression (10) comportant une mémoire électronique volatile (74), ladite image d'entrée étant représentée par des données d'image, sous forme d'un flux de données, comprenant une pluralité de bits successifs regroupés en des premiers ensembles de bits (411A, 411B, 411C),
chaque ensemble comprenant n bits, comprenant les étapes consistant à :

coder (402) lesdits premiers ensembles de bits en des seconds ensembles de bits (00, 01, 10, 11), chacun des seconds ensembles de bits présentant moins de bits (n - m) que chacun des premiers ensembles de bits, m étant le nombre des bits rejetés dans chaque ensemble de bits en tant que résultat dudit codage,
mémoriser (406) le flux de bits codé dans la mémoire électronique volatile (74) avec un espace de mémoire économisé en tant que résultat de la réduction de la taille de chacun des premiers ensembles de bits,
analyser le flux de bits codé mémorisé en définissant un second ensemble de bits central disposé entre un second ensemble de bits de gauche et un second ensemble de bits de droite, respectivement, afin de générer un signal correspondant affecté audit second ensemble de bits central et déterminé en comparant les intensités dudit second ensemble de bits de gauche et dudit second ensemble de bits de droite,
reconstituer le flux de bits codé mémorisé en convertissant les seconds ensembles de bits en troisièmes ensembles de bits, chacun desdits troisièmes ensembles de bits comportant à nouveau n bits, les bits dudit ensemble de bits central étant agencés sur la base dudit signal de sorte que les bits représentant une couleur noire dudit bit central sont associés à celui desdits ensembles de bits voisins de gauche ou de droite qui possèdent l'intensité la plus grande, et
fournir en sortie une représentation en image du flux de bits reconstitué.

2. Procédé selon la revendication 1, dans lequel chacun des premier et second ensembles de bits correspond à un pixel et les pixels sont disposés dans une pluralité de lignes de balayage, dans lequel ladite étape d'analyse est exécutée sur chaque ligne de balayage.

3. Procédé selon la revendication 2, comprenant en outre l'étape consistant à fournir une table de consultation (415), dans une seconde mémoire électronique (434), la table de consultation comprenant

une pluralité de paires d'intensités, chaque paire étant mappée sur l'un desdits signaux, respectivement, et dans lequel :

ladite étape d'analyse comprend la mise en correspondance des intensités respectives des pixels à gauche et à droite d'un pixel central avec l'une des paires d'intensités dans la table de consultation afin d'obtenir ledit signal correspondant.

4. Procédé selon la revendication 3, dans lequel, lorsque l'intensité du pixel de gauche est la même que celle du pixel de droite, ladite étape d'analyse analyse :

au moins une ligne de balayage voisine (428) avec un quatrième pixel disposé entre un cinquième pixel et un sixième pixel à une position correspondant à la position desdits pixels du centre, de gauche et de droite, respectivement et en examinant les intensités respectives des cinquième et sixième pixels, et
en déterminant ledit signal du pixel central conformément aux signaux obtenus en analysant la au moins une ligne de balayage voisine.

5. Procédé selon l'une des revendications 1 à 4, dans lequel ladite étape de sortie comprend l'impression de l'image, sur un substrat, avec un moteur d'impression (20).

6. Procédé selon l'une des revendications 1 à 5, dans lequel ladite étape de codage comprend le codage du flux de bits avec un dispositif de traitement d'image (22).

7. Dispositif destiné à traiter une image d'entrée représentée par des données d'image sous forme d'un flux de données comprenant une pluralité de bits successifs regroupés en des premiers ensembles de bits (411A, 411B, 411C), chaque ensemble de bits comprenant n bits, comprenant :

un dispositif destiné à coder (62) lesdits premiers ensembles de bits en des seconds ensembles de bits (00, 01, 10, 11), chacun des seconds ensembles de bits comportant moins de bits (n - m) que chacun des premiers ensembles de bits, m étant le nombre des bits rejetés dans chaque ensemble de bits en tant que résultat dudit codage,
une mémoire électronique volatile (74) destinée à mémoriser (406) le flux de bits codé dans la mémoire électronique volatile (74), de l'espace de la mémoire étant économisé en tant que résultat de la réduction d'une taille de chacun des premiers ensembles de bits,
un analyseur de flux de bits (415, 432, 440 ; 434) destiné à analyser le flux de bits codé mémorisé en définissant un second ensemble de bits central disposé entre un second ensemble de bits de gauche et un second ensemble de bits de droite, respectivement afin de générer un signal correspondant affecté audit second ensemble de bits central et déterminé en comparant les intensités dudit second ensemble de bits de gauche et dudit second ensemble de bits de droite,
un circuit de reconstitution (64 ; 20) destiné à reconstituer le flux de bits codé mémorisé en convertissant les seconds ensembles de bits en des troisièmes ensembles de bits, chacun desdits troisièmes ensembles de bits comportant à nouveau n bits, les bits dudit ensemble de bits central étant agencés sur la base dudit signal, de sorte que les bits représentant une couleur noire dudit ensemble de bits central sont associés à celui des ensembles de bits voisins de gauche ou de droite possédant l'intensité la plus grande, et
un dispositif de sortie (20 ; 51, 28) destiné à fournir en sortie une représentation en image du flux de bits reconstitué.

8. Dispositif de traitement d'image selon la revendication 7, dans lequel chacun des premier et second ensembles de bits correspond à un pixel et les pixels sont disposés dans une pluralité de lignes de balayage (411, 428, 438).

9. Dispositif de traitement d'image selon la revendication 8, dans lequel ledit analyseur de flux de bits (415, 440 ; 434) comprend une table de consultation (LUT ; 415), dans une seconde mémoire électronique (432), la table de consultation comprenant une pluralité de paires d'intensités, chaque paire étant mappée sur l'un desdits signaux, respectivement, et dans lequel les intensités respectives des pixels à gauche et à droite d'un pixel central sont mises en correspondance dans l'analyseur de flux de bits avec l'une des paires d'intensités de la table de consultation afin d'obtenir le signal correspondant.

10. Dispositif de traitement d'image selon la revendication 9, dans lequel, lorsque l'intensité du pixel de gauche est la même que celle du pixel de droite, ledit analyseur de flux de bits analyse au moins une ligne de balayage voisine (428) avec un quatrième pixel disposé entre un cinquième pixel et un sixième pixel à une position correspondant à la position desdits pixels du centre, de gauche et de droite, respectivement, examine les intensités respectives des cinquième et sixième pixels, et détermine ledit signal du pixel central conformément aux signaux obtenus en analysant ladite au moins une ligne de balayage voisine.

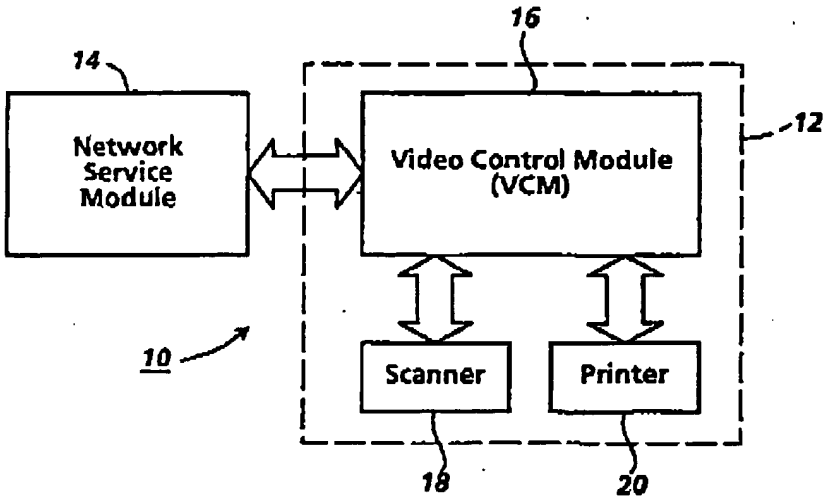

FIG. 1

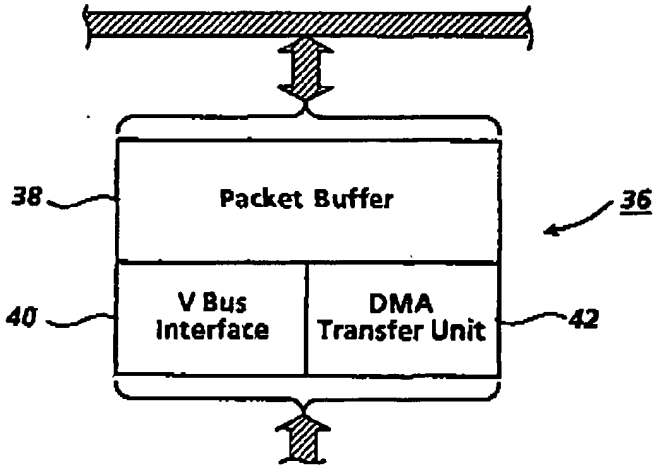

FIG. 3

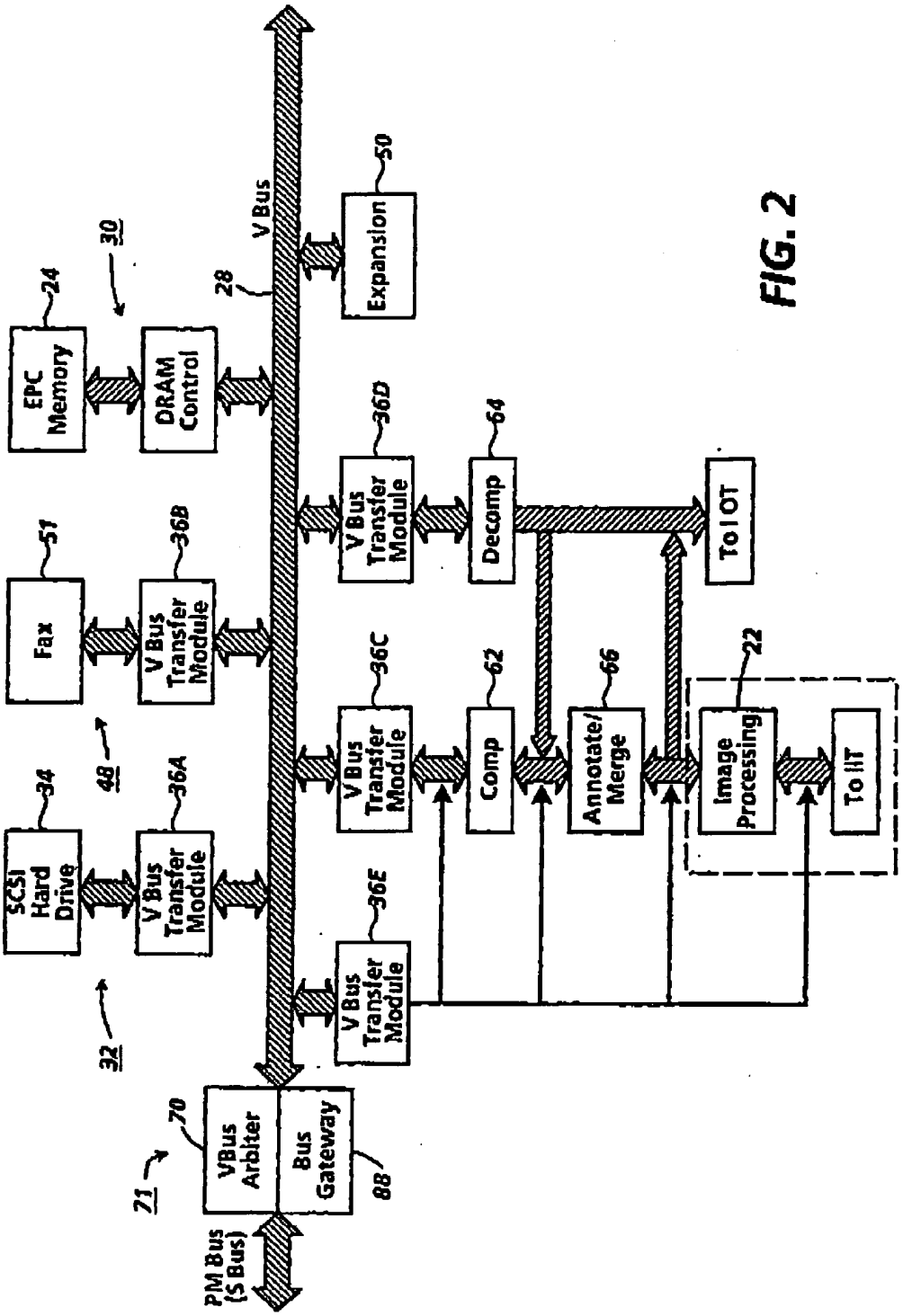

FIG. 2

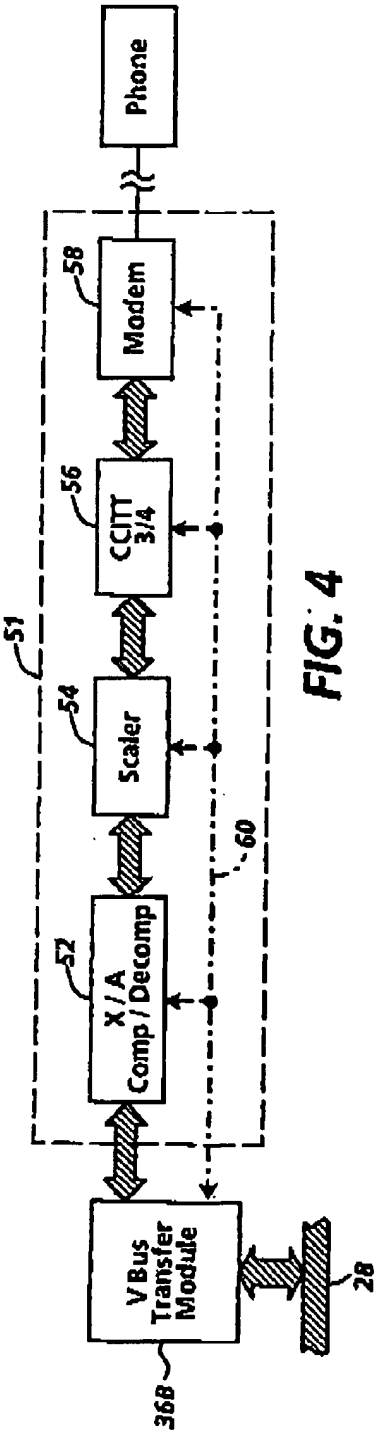

FIG. 4

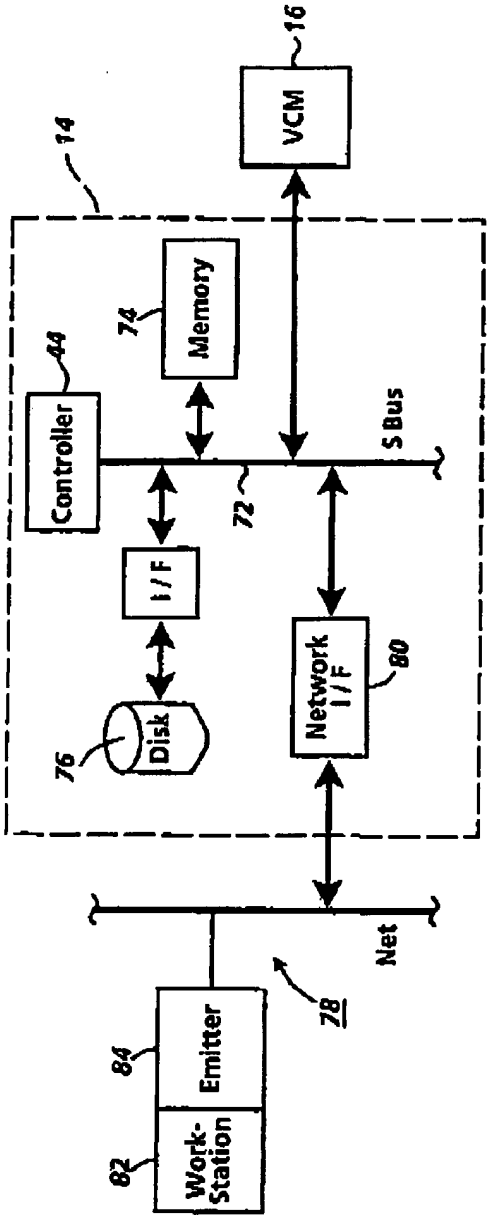

FIG. 5

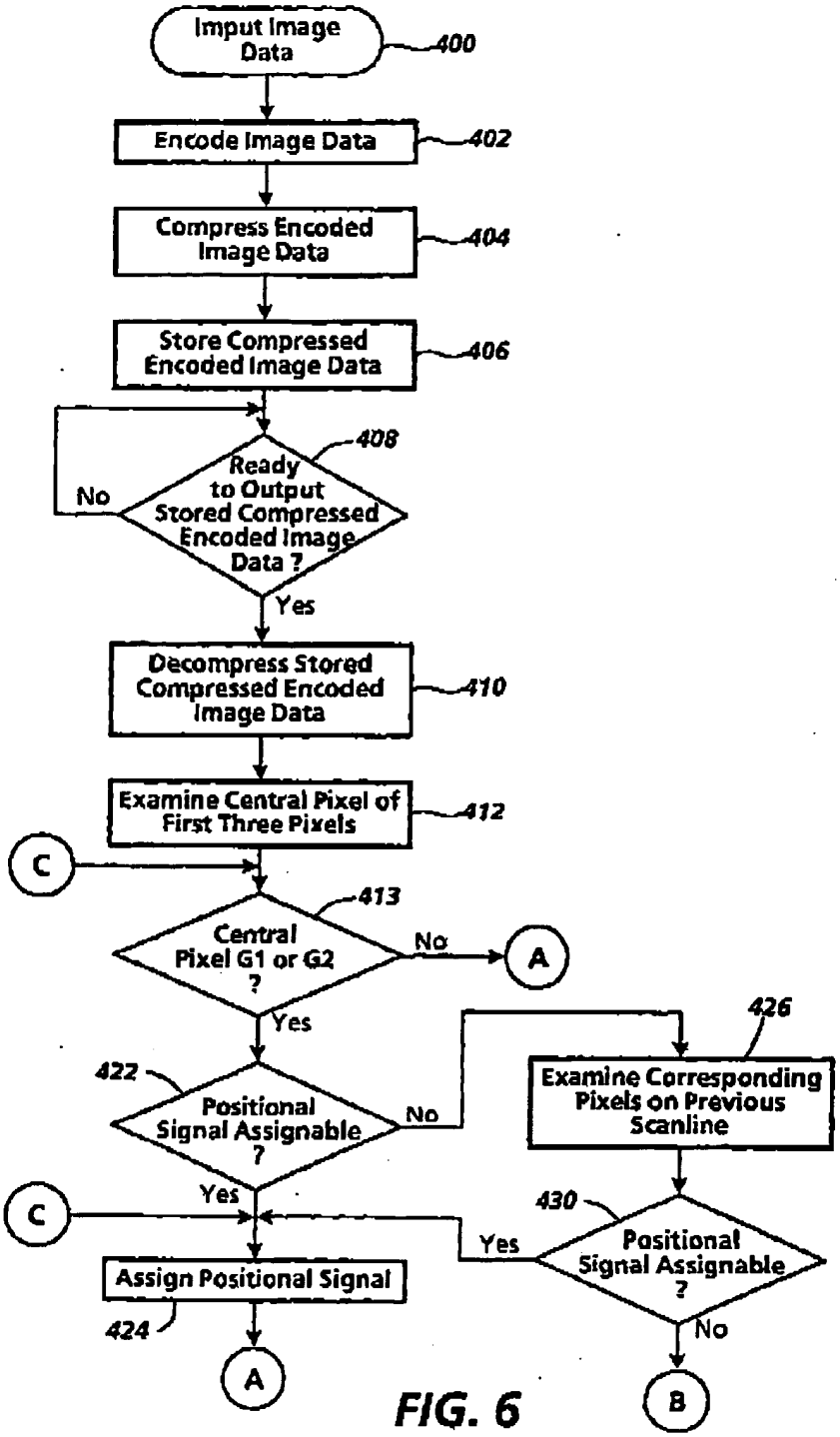

FIG. 6

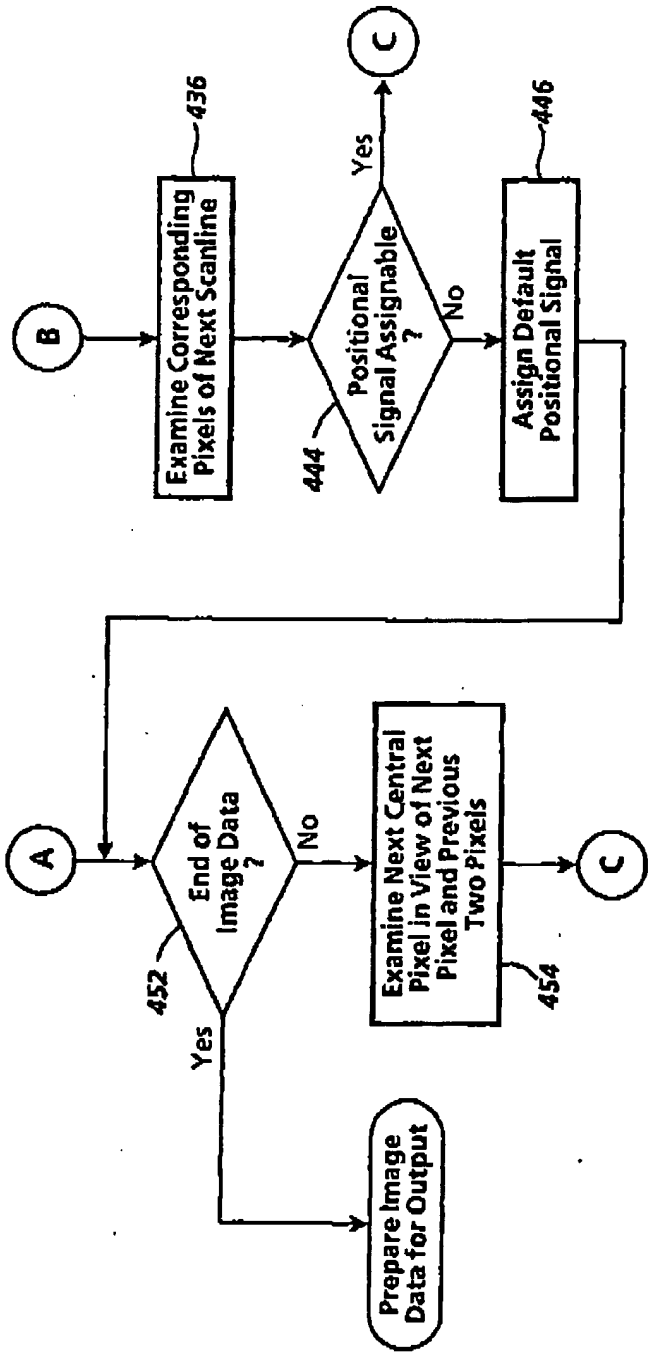

FIG. 7

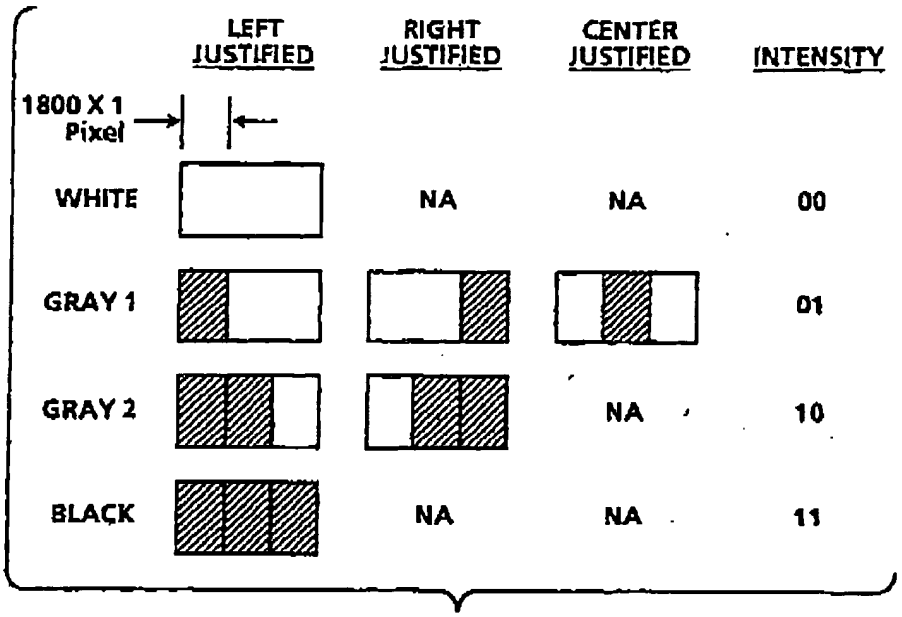

FIG. 8

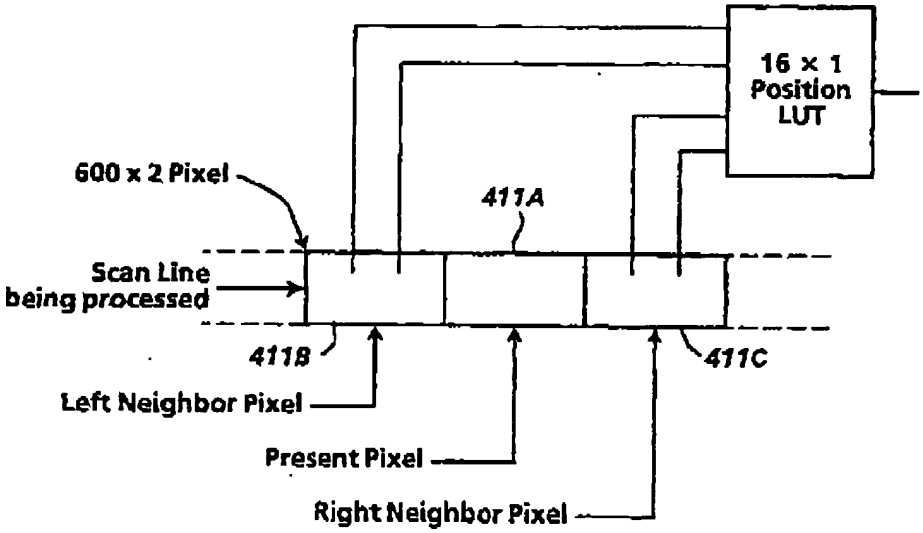

FIG. 9

Left Neighbor Pixel	Present Pixel	Right Neighbor Pixel	POSITION	VALUE
W		W	L	1
W		G1	R	0
W		G2	R	0
W		B	R	0
G1		W	L	1
G1		G1	R	0
G1		G2	R	0
G1		B	R	0
G2		W	L	1
G2		G1	L	1
G2		G2	L	1
G2		B	R	0
B		W	L	1
B		G1	L	1
B		G2	L	1
B		B	R	0

415

FIG. 10

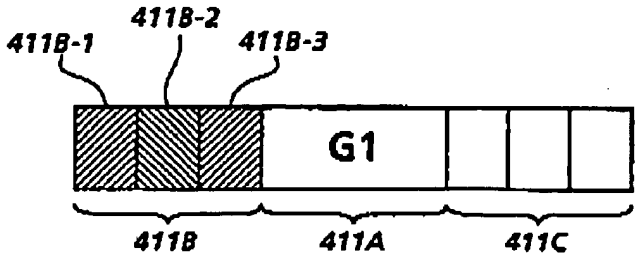

FIG. 11A

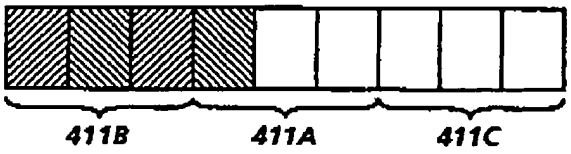

FIG. 11B

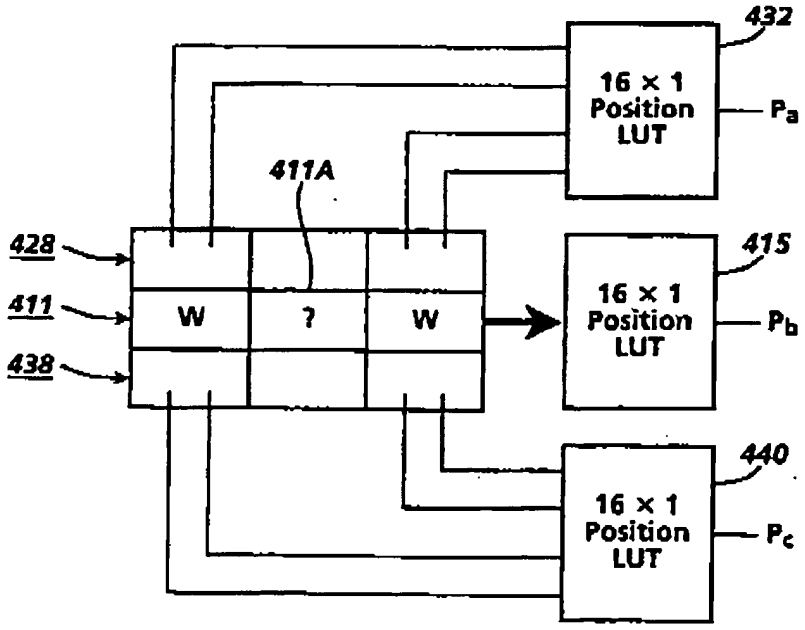

FIG. 12

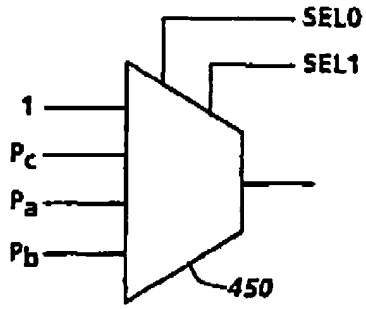

FIG. 13

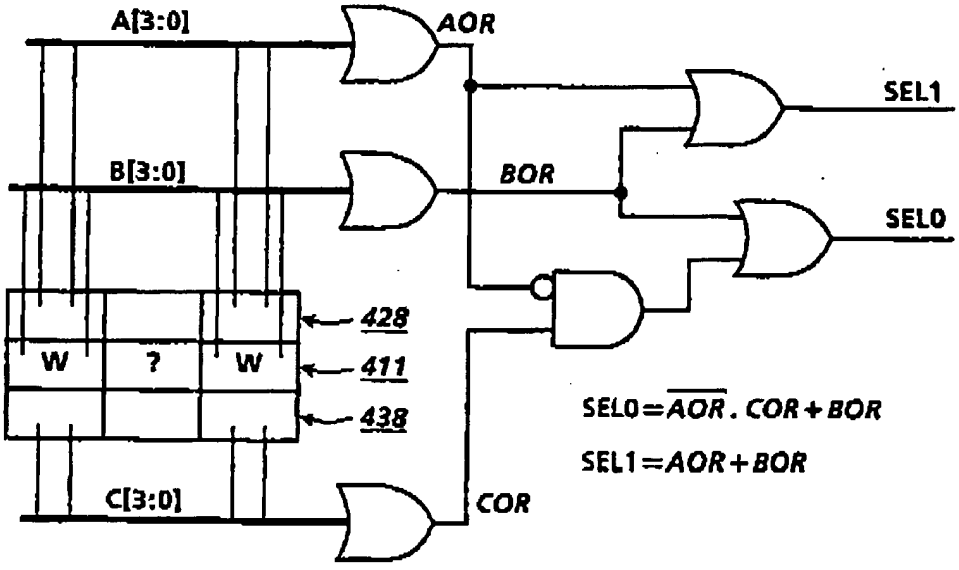

FIG. 14

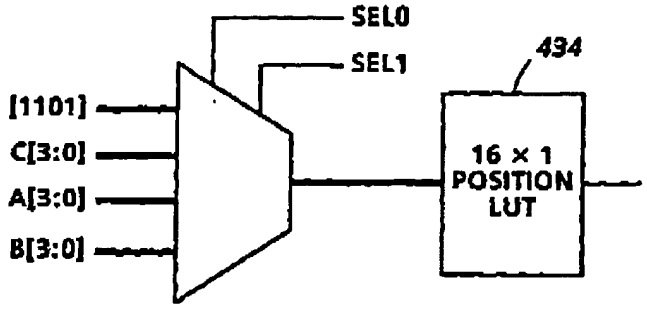

FIG. 15

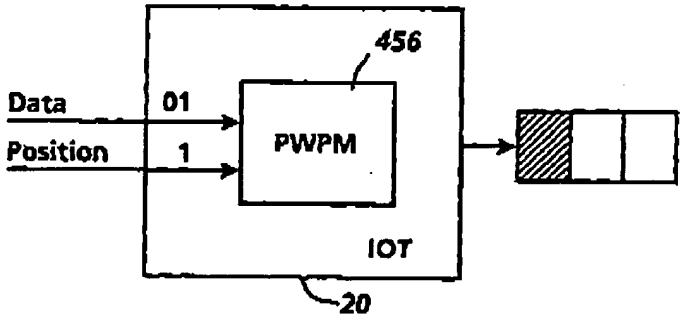

FIG. 16

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(54) Apparatus and method for encoding and reconstructing image data

Vorrichtung und Verfahren zur Kodierung und Wiederherstellung von Bilddaten

Appareil et procédé pour le codage et la reconstruction de données d'image

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Description

[0001] The present invention relates generally to a technique for both storing and outputting image data in a printing system and, more particularly, to an apparatus and method in which image data, from an input image, is encoded and the resulting encoded bitstream is then reconstructed.

[0002] Electronic printing systems typically include an input section, sometimes referred to as an input image terminal ("IIT"), a controller, sometimes referred to as an electronic subsystem ("ESS") and an output section or print engine, sometimes referred to as an image output terminal ("IOT"). In one type of electronic printing system, manufactured by Xerox® Corporation, known as the DocuTech® electronic printing system, a job can be inputted to the IIT from, among other sources, a network or a scanner. An example of an IIT with both network and scanner inputs is found in US-A-5,170,340.

[0003] It is known that output of an image can be enhanced significantly through use of a high addressability output device. For example, through employment of a printing machine with a capability of storing or buffering scanned data prepared at a resolution of 600 x 3 spi, a corresponding output of 1800 x 1 spi can be obtained. While this sort of output is desirable, storing image data at 600 x 3 spi, even for short time periods, can be burdensome on a printing machine with relatively limited volatile or system memory, such as some of the digital printing systems discussed above. While various ones of the above printing systems advantageously exploit disk storage, in conjunction with system memory, it is, for purposes of outputting a job, necessary to store or buffer the job in system memory. Moreover, even in a digital printing machine which takes advantage of disk, storage of an image is achieved, commonly, by "funneling" the image through the system memory on its way to disk. Such funneling process can "clog" up system memory readily when the image is relatively complex. It would be desirable to store or buffer a job in system memory of a high addressability printing machine, at a first resolution, and output it at a second resolution where the first resolution is significantly less than the second resolution.

[0004] In one example, storing or buffering a job at less than 600 x 3 spi is accomplished by discarding image-related information, i.e. image data. This discarding of image data can lead to a degradation of image quality when reproducing the remaining image data. It would be desirable to provide a technique in which at least a part of the discarded image data could be reconstructed so that image degradation is minimized.

[0005] It is an object of the present invention to provide a method and apparatus embodying such a technique.

[0006] This object is solved by a method according to claim 1 and an image processing apparatus according to claim 7.

[0007] Preferred embodiments are the subject-matters of the dependent claims.

[0008] The invention will become apparent from the following description, the description being used to illustrate a preferred embodiment of the invention when read in conjunction with the accompanying drawings, in which:-

Figure 1 is a block diagram depicting a multifunctional, network adaptive printing machine;
Figure 2 is a block diagram of a video control module for the printing machine of Figure 1;
Figure 3 is a block diagram of a transfer module used in conjunction with the printing machine of Figure 2;
Figure 4 is a block diagram of a facsimile card used in conjunction with the printing machine of Figure 2;
Figure 5 is a block diagram of a network controller for the printing machine of Figure 1;
Figures 6 and 7 represent a flow diagram depicting a technique for encoding and reconstructing an input image;
Figure 8 is a schematic representation depicting an encoding scheme of the present technique;
Figure 9 is a schematic representation of an analyzing circuit used in a reconstruction arrangement of the present technique;
Figure 10 is a schematic representation of the contents of a look-up table of Figure 9;
Figures 11A and 11B are schematic, partial representations of scanlines, the schematic, partial representations being employed to illustrate one aspect of the present technique;
Figure 12 is a schematic representation of another analyzing circuit used in conjunction with one aspect of the present technique;
Figure 13 is a schematic representation of a multiplexing arrangement used in conjunction with the analyzing circuit of Figure 12;
Figure 14 is a schematic representation of a select circuit used to generate the select signals for the multiplexing arrangement of Figure 13;
Figure 15 is schematic representation of another multiplexing arrangement usable with the analyzing circuit of Figure 12; and
Figure 16 is a schematic representation of a printer with a pulse width position modulator, the pulse width position modulator being responsive to encoded/reconstructed data generated in accordance with the present technique.

[0009] Referring to Figure 1, a multifunctional, network adaptive printing system is designated by the numeral 10. The printing system 10 includes a printing machine 12 operatively coupled with a network service module 14. The printing machine 12 includes an electronic subsystem 16, referred to as a video control module (VCM), communicating with a scanner 18 and a

printer 20. In one example, the VCM 16, which will be described in further detail below, coordinates the operation of the scanner and printer in a digital copying arrangement. In a digital copying arrangement, the scanner 18 (also referred to as image input terminal (IIT)) reads an image on an original document by using a CCD full width array and converts analog video signals, as gathered, into digital signals. In turn, an image processing system 22 (Figure 2), associated with the scanner 18, executes signal correction and the like, converts the corrected signals into multi-level signals (e.g. binary signals), compresses the multi-level signals and preferably stores the same in electronic precollation (EPC) memory 24.

[0010] Referring again to Figure 1, the printer 20 (also referred to as image output terminal (IOT)) preferably includes a xerographic print engine. In one example, the print engine has a multi-pitch belt (not shown) which is written on with an imaging source, such as a synchronous source (e.g. laser raster output scanning device) or an asynchronous source (e.g. LED print bar). In a printing context, the multi-level image data is read out of the EPC memory 24 (Figure 2) while the imaging source is turned on and off, in accordance with the image data, forming a latent image on the photoreceptor. In turn, the latent image is developed with, for example, a hybrid jumping development technique and transferred to a print media sheet. Upon fusing the resulting print, it may be inverted for duplexing or simply outputted. It will be appreciated by those skilled in the art that the printer can assume other forms besides a xerographic print engine without altering the concept upon which the disclosed embodiment is based. For example, the printing system 10 could be implemented with a thermal ink jet or ionographic printer.

[0011] Referring specifically to Figure 2, the VCM 16 is discussed in further detail. The VCM 16 includes a video bus (VBus) 28 with which various I/O, data transfer and storage components communicate. Preferably, the VBus is a high speed, 32 bit data burst transfer bus which is expandable to 64 bit. The 32 bit implementation has a sustainable maximum bandwidth of approximately 60 MBytes/sec. In one example, the bandwidth of the VBus is as high as 100 MBytes/sec.

[0012] The storage components of the VCM reside in the EPC memory section 30 and the mass memory section 32. The EPC memory section includes the EPC memory 24, the EPC memory being coupled with the VBus by way of a DRAM controller 33. The EPC memory, which is preferably DRAM, provides expansion of up to 64 MBytes, by way of two high density 32 bit SIMM modules. The mass memory section 32 includes a SCSI hard drive device 34 coupled to the VBus by way of a transfer module 36a. As will appear, other I/O and processing components are coupled respectively to the VBus by way of transfer modules 36. It will be appreciated that other devices (e.g. a workstation) could be coupled to the VBus by way of the transfer module 36a through use of a suitable interface and a SCSI line.

[0013] Referring to Figure 3, the structure of one of the transfer modules 36 is discussed in further detail. The illustrated transfer module of Figure 3 includes a packet buffer 38, a VBus interface 40 and DMA transfer unit 42 . The transfer module 36, which was designed with "VHSIC" Hardware Description Language (VHDL), is a programmable arrangement permitting packets of image data to be transmitted along the VBus at a relatively high transfer rate. In particular, the packet buffer is programmable so that the segment or packet can be varied according to the available bandwidth of the VBus. In one example, the packet buffer can be programmed to handle packets of up to 64 Bytes Preferably, the packet size would be reduced for times when the VBus is relatively busy and increased for times when activity on the bus is relatively low.

[0014] Adjustment of the packet size is achieved with the VBus interface 40 and a system controller 44 (Figure 5). Essentially, the VBus interface is an arrangement of logical components, including, among others, address counters, decoders and state machines, which provides the transfer module with a selected degree of intelligence. The interface 40 communicates with the system controller to keep track of desired packet size and, in turn, this knowledge is used to adjust the packet size of the packet buffer 38, in accordance with bus conditions. That is, the controller, in view of its knowledge regarding conditions on the VBus 28, passes directives to the interface 40 so that the interface can adjust packet size accordingly. Further discussion regarding operation of the transfer module 36 is provided below

[0015] More particularly, each DMA transfer unit employs a conventional DMA transfer strategy to transfer the packets. In other words, the beginning and end addresses of the packet are used by the transfer unit in implementing a given transfer. When a transfer is complete, the interface 40 transmits a signal back to the system controller 44 so that further information, such as desired packet size and address designations, can be obtained.

[0016] Referring to Figures 1 and 2, three I/O components are shown as being coupled operatively to the VBus 28, namely a FAX module 48, the scanner or IIT 18, and the printer or IOT 20; however, it should be recognized that a wide variety of components could be coupled to the VBus by way an expansion slot 50. Referring to Figure 4, an implementation for the FAX module, which is coupled to the VBus 28 by way of transfer module 36b, is discussed in further detail. In the preferred embodiment, a facsimile device (FAX) 51 includes a chain of components, namely a section 52 for performing Xerox adaptive compression/decompression, a section 54 for scaling compressed image data, a section 56 for converting compressed image data to or from CCITT format, and a modem 58, preferably manufactured by Rockwell Corporation, for transmitting CCITT formatted data from or to a telephone, by way of a conventional

communication line.

[0017] Referring still to Figure 4, each of the sections 52, 54 and 56 as well as modem 58 are coupled with the transfer module 36b by way of a control line 60. This permits transfers to be made to and from the FAX module 46 without involving a processor. As should be understood, the transfer module 36b can serve as a master or slave for the FAX module in that the transfer module can provide image data to the FAX for purposes of transmission or receive an incoming FAX. In operation, the transfer module 36b reacts to the FAX module in the same manner that it would react to any other I/O component. For example, to transmit a FAX job, the transfer module 36b feeds packets to the section 52 through use of the DMA transfer unit 42 and, once a packet is fed, the transfer module transmits an interrupt signal to the system processor 44 requesting another packet. In one embodiment, two packets are maintained in the packet buffer 38 so that "ping-ponging" can occur between the two packets. In this way, the transfer module 36b does not run out of image data even when the controller cannot get back to it immediately upon receiving an interrupt signal.

[0018] Referring again to Figure 2, the IIT 18 and IOT 20 are operatively coupled to the VBus 28 by way of transfer modules 36c and 36d. Additionally, the IIT 18 and the IOT 20 are operatively coupled with a compressor 62 and a decompressor 64, respectively. The compressor and decompressor are preferably provided by way of a single module that employs Xerox adaptive compression devices. Xerox adaptive compression devices have been used for compression/decompression operations by Xerox Corporation in its DocuTech® printing system. In practice, at least some of the functionality of the transfer modules is provided by way of a 3 channel DVMA device, which device provides local arbitration for the compression/decompression module.

[0019] As further illustrated by Figure 2, the scanner 18, which includes the image processing section 22, is coupled with an annotate/merge module 66. Preferably the image processing section includes one or more dedicated processors programmed to perform various desired functions, such as image enhancement, thresholding/screening, rotation, resolution conversion and TRC adjustment. The selective activation of each of these functions can be coordinated by a group of image processing control registers, the registers being programmed by the system controller 44. Preferably, the functions are arranged along a "pipeline" in which image data is inputted to one end of the pipe, and image processed image data is outputted at the other end of the pipe. To facilitate throughput, transfer module 36e is positioned at one end of the image processing section 22 and transfer module 36c is positioned at another end of the section 22. As will appear, positioning of transfer modules 36c and 36e in this manner greatly facilitates the concurrency of a loopback process.

[0020] Referring still to Figure 2, arbitration of the various bus masters of the VCM 16 is implemented by way of a VBus arbiter 70 disposed in a VBus arbiter/bus gateway 71. The arbiter determines which bus master (e.g. FAX module, Scanner, Printer, SCSI Hard Drive, EPC Memory or Network Service Component) can access the VBus at one given time. The arbiter is made up of two main sections and a third control section. The first section, i.e., the "Hi-Pass" section, receives input bus requests and current priority selection, and outputs a grant corresponding to the highest priority request pending. The current priority selection input is the output from the second section of the arbiter and is referred to as "Priority Select". This section implements priority rotation and selection algorithm. At any given moment, the output of the logic for priority select determines the order in which pending requests will be serviced. The input to Priority Select is a register which holds an initial placement of devices on a priority chain. On servicing requests, this logic moves the devices up and down the priority chain thereby selecting the position of a device's next request. Control logic synchronizes the tasks of the Hi-Pass and the Priority Select by monitoring signals regarding request/grant activity. It also prevents the possibility of race conditions.

[0021] Referring to Figure 5, the network service module 14 is discussed in further detail. As will be recognized by those skilled in the art, the architecture of the network service module is similar to that of a known "PC clone". More particularly, in the preferred embodiment, the controller 44, which preferably assumes the form of a SPARC processor, manufactured by Sun Microsystems, Inc., is coupled with a standard SBus 72. In the illustrated embodiment of Figure 5, a host memory 74, which preferably assumes the form of DRAM, and a SCSI disk drive device 76 are coupled operatively to the SBus 72. While not shown in Figure 5, a storage or I/O device could be coupled with the SBus with a suitable interface chip. As further shown in Figure 5, the SBus is coupled with a network 78 by way of an appropriate network interface 80. In one example, the network interface includes all of the hardware and software necessary to relate the hardware/software components of the controller 44 with the hardware/software components of the network 78. For instance, to interface various protocols between the network service module 14 and the network 78, the network interface could be provided with, among other software, Netware® from Novell Corp.

[0022] In one example, the network 78 includes a client, such as a workstation 82 with an emitter or driver 84. In operation, a user may generate a job including a plurality of electronic pages and a set of processing instructions. In turn, the job is converted, with the emitter, into a representation written in a page description language, such as PostScript. The job is then transmitted to the controller 44 where it is interpreted with a decomposer, such as one provided by Adobe Corporation.

[0023] Referring again to Figure 2, the network service module 14 is coupled with the VCM 16 via a bus gate-

way 88 of the VBus arbiter/bus gateway 71. In one example, the bus gateway comprises a field programmable gate array provided by XILINX corporation. The bus gateway device provides the interface between the host SBus and the VCM VBus. It provides VBus address translation for accesses to address spaces in the VBus real address range, and passes a virtual address to the host SBus for virtual addresses in the host address range. A DMA channel for memory to memory transfers is also implemented in the bus gateway. Among other things, the bus gateway provides seamless access between the VBus and SBus, and decodes virtual addresses from bus masters, such as one of the transfer modules 36, so that an identifier can be obtained from a corresponding slave component. It will be appreciated by those skilled in the art that many components of the printing system 10 are implemented in the form of a single ASIC.

[0024] Referring to Figures 2, 3 and 5, further discussion regarding DMA transfer of each of the transfer modules 36 is provided. In particular, in one example, the images of a job are stored in the host memory 74 as a series of blocks which are stored in the EPC memory 24. Preferably, each block comprises a plurality of packets. In operation, one of the transfer modules 36 is provided, by the controller 44, with the beginning address of a block and the size of the block. In turn, for that block, the transfer module 36 effects a packet tranfer and increments/decrements a counter. This procedure is repeated for each packet of the block until the interface 40 determines, by reference to the counter, that the last packet of the block has been transferred. Typically, for each stored image, several blocks are transferred, in a packet-by-packet manner, as described immediately above.

[0025] Referring to Figures 2, 5, 6 and 7, an image processing technique, appropriate for use with printing system 10, is discussed. In the illustrated embodiment of Figure 6, input image data, for a given input image, is, at step 400, inputted to image processing section 22 (Figure 2). In one mode of operation, the inputted image data is obtained at the scanner 18. More particularly, a document is scanned and 2^x bits of gray data is provided in the form of a bitstream. In turn, the gray data is thresholded so that the image is expressed as n bits of data where n is less than 2^x. In one example, the given input image is processed at 600 x 3 spi so that n = 3 and a resulting output, with a resolution of 1800 x 1 spi, can be obtained. It has been found, however, as explained in further detail below, that, for this example, storage can be optimized and an output resolution of 1800 x 1 spi obtained even when the value of n is less than 3. As will appear, the present technique is applicable for inputs and outputs of various resolutions, and image data can be obtained from a wide range of input sources without affecting the concept underlying the disclosed embodiment.

[0026] In accordance with the preferred technique, at step 402, image data is encoded. Referring to the illustrated embodiment of Figure 8, n bits are described with n - m bits where each m bit represents, as explained in further detail below, positional information. In one example, three bits are described generally with two bits, or, stated alternatively, at one of four levels. It follows from the illustration of Figure 8, that in a high addressability approach, each 600 x 2 pixel can be encoded so as to simulate 1800 x 1 data. Normally, three bits would be required to describe three pixels at 1800 x 1 spi, but in the illustrated scheme of Figure 8, only two bits, designated by the term "intensity", are required to describe a group of three 1800 x 1 spi pixels. That is a 600 x 2 spi pixel, with an intensity of 00, is equivalent to three white pixels at 1800 x 1 output, a 600 x 2 spi pixel, with an intensity of 01, is equivalent to one black pixel and two white pixels, at 1800 x 1 spi, and so on.

[0027] It should be recognized, nonetheless that certain image-related information is lost by the encoding scheme of Figure 8 in that the pixels labeled as "GRAY1" and "GRAY2" cannot be fully described by just two bits. In other words, use of only two bits does not indicate whether the black pixel is left justified, right justified or center justified. Effectively, as explained in further detail below, this information can be provided, via a reconstruction step.

[0028] Referring again to Figures 2 and 6, preferably, an encoded bitstream is compressed, with compressor 62 (step 404) and then stored in EPC memory 24 (step 406). The compressed, encoded bitstream is, via step 408, held in the EPC memory until it is either copied to disk 34 (step not shown) or outputted to an appropriate output device, such as the printer 20. When it is time to output the stored encoded bitstream, decompression is effected, via step 410, with the decompressor 64. As will be appreciated from the discussion above, movement of data between the image processing section, compressor, EPC memory and the decompressor, is facilitated with the transfer modules 36.

[0029] In anticipation of outputting the image data, the corresponding bitstream is analyzed, per step 412, with a bitstream analyzing arrangement. Referring generally to Figures 9-13, an example of a reconstruction scheme, with a bitstream analyzer is illustrated. It will be appreciated by those skilled in the art that operation of the bitstream analyzer can be implemented with a suitable processor. Moreover, the image assumes the form of a bitmap with a plurality of scanlines.

[0030] Referring to Figures 6, 8 and 9, when a present or central pixel 411a corresponds with three white or three black pixels, then the central pixel can be described completely with two bits. In the case of an all white or all black central pixel 411a, the process proceeds to step 452 (Figure 7). When, however, the central pixel is GRAY1 (i.e. "G1") or GRAY2 (i.e. "G2") pixel (step 413), then the central pixel cannot be described with two bits.

[0031] Referring specifically to Figure 9, a preferred

approach for interpreting G1 and G2 central pixels is discussed. In the preferred approach, each pixel for a given input bitstream is read for purposes of comparing bit pairs representative of "neighboring" or "framing" pixels with the entries of a 16 x 1 look-up table. More particularly, each central pixel 411a is disposed intermediate of a left neighbor pixel 411b and a right neighbor pixel 411c. In one example of operation, the respective bit pairs of the left neighbor and the right neighbor, for each G or G2 pixel, are compared to each of sixteen bit pairs in the look-up table 415 of Figure 10. In turn, a match is obtained and a corresponding positional signal or value is assigned to the central or present pixel.

[0032] The positional signal of the illustrated look-up table facilitates a reconstruction of the bit discarded during the encoding of the image data. More particularly, it is known that, in a typical black and white image, black pixels tend to group together. Accordingly, this knowledge can be used in reconstructing the present pixel of Figure 8 when that pixel assumes the form of the G1 pixel or the G2 pixel. It stands to reason that the gray part of a G1 or G2 central pixel would tend to associate with the neighboring pixel having the greatest intensity.

[0033] This approach can be best understood by reference to an example of Figures 11A and 11B. The pixel 411b, which has an intensity of 11, is referred to, in the look-up table 415 (Figure 10), as "B" and the pixel 411c, which has an intensity of 00, is referred to, in the look-up table, as "W". As indicated by the look-up table, the position of the gray pixel in the present pixel is left justified (Figure 8) so that the one black pixel of the pixel 411a is grouped with the black pixels 411b-1, 411b-2 and 411b-3 of pixel 411b. It will be appreciated that while the current methodology groups black pixels, in another approach, white pixels could be grouped together.

[0034] The approach discussed above assumes that the left neighbor pixel and the right neighbor pixel have different intensities. When this assumption holds true, the process proceeds to step 422 (Figure 6), and then step 424 where a positional signal of "0" or "1" is assigned to the central or present pixel 411A. It should be appreciated that a single bit cannot designate each case for a GRAY1 pixel in that an 1800 x 1 pixel (Figure 8) can assume one of three positions. The present technique assumes that the 1800 x 1 pixel is either left or right justified. In another embodiment, center justification would be accommodated for by using two bits to describe the positional signal. It will be recognized that use of two bits to describe justification provides additional flexibility to the current technique.

[0035] Referring to Figure 10, for the case in which the left neighbor pixel/right neighbor pixel pair is W-W, an ambiguity exists because there is no reason, based on a single scanline analysis, for justifying the gray part of the present pixel to the left or to the right. In the illustrated embodiment of Figure 10, the positional signal or value of the the four cases is assigned on the basis of empirical observations regarding image data output.

Referring generally to Figures 12-14, an approach for optimizing the present technique, when the left neighbor pixel/right neighbor pixel pair is W-W, is discussed.

[0036] Referring conjunctively to Figures 6 and 12, when the present or central pixel 411a of a scanline 411 being processed cannot be assigned a positional signal, because the respective intensities of the left neighbor pixel and the right neighbor pixel are white (step 426), a corresponding two pixels of a previous scanline 428 are examined (step 430) with the bitstream analyzer. To effect the examination, a second 16 x 1 look-up table 432, identical to the one of Figures 10 and 12, namely look-up table 415, is employed. If a match is found in the second look-up table, and the match does not relate to a bit pair in which the intensities are the same (e.g. the intensities are W-W), then a positional signal is obtained in the same manner as described for step 424.

[0037] Referring to Figures 17 and 12, if the positional signal for the present pixel cannot be designated, by reference to the previous scanline, because the respective intensities of the corresponding pixels of the previous scanline are, for example, both white, then, via step 436, the intensities of a corresponding two pixels of a next scanline 438 are examined with a third look-up table 440, which third look-up table is identical in content to the first look-up table 434. If a match is found in the third look-up table, and the match does not relate to a bit pair in which the intensities are each white, then a positional signal is obtained in the same manner as described for step 424. If a match cannot be made on the basis of examining any of the scanlines 425, 428 or 438, then, via steps 444, 446, default positional value is, via step 446, assigned.

[0038] In the illustrated embodiment of Figures 6, 7 and 12, the three scanlines are analyzed simultaneously to determine what the positional signal of the present pixel should be Preferably, one of a plurality of output signals from the look-up tables 415, 432 and 440 is then chosen with a 4 to 1 multiplexer 450 (Figure 13), which multiplexer is controlled by selected signals designated as "SEL0" and SEL1". Referring to Figure 14, an implementation for generating the select signals is shown. Referring conjunctively to Figures 13 and 14, when the respective signals of SEL0 and SEL1 are 1 and 1, the positional signal of look-up table 415 is permitted to pass through a multiplexer 450. When the respective signals of SEL0 and SEL1 are 1 and 0, the positional signal of look-up table 432 is permitted to pass through the multiplexer 450. When the respective signals of SEL0 and SEL1 are 0 and 1, the positional signal of look-up table 440 is permitted to pass through the multiplexer 450. In a default case, namely when the respective signals of SEL0 and SEL1 are 0 and 0, a preassigned signal, e.g. a 1, is permitted to pass through the multiplexer 450. It will be appreciated that the preassigned signal may be assigned, for example, on the basis of empirical data.

[0039] Referring to Figure 15, in another embodiment, the position signal for the present pixel 423 could be ob-

tained through the use of an arrangement with just one of the look-up tables 415, 434 or 440 and the multiplexer 450. More particularly, in this other embodiment, the bits corresponding to each of the framing or neighboring pixels of scanlines 411, 428 and 438, along with a suitable set of default bits, is transmitted to the four inputs of the multiplexer 450. Through use of appropriate select signals, from the select circuit of Figure 14, one of the bit sets is permitted to pass through the multiplexer, and, in turn, that bit set is processed with the look-up table.

[0040] Referring again to Figure 7, subsequent to the assignment of each positional signal, a check is performed, at step 352, to determine if all of the image data for a given input image has been processed. If an end to the image data has not been reached, then the neighboring pixels of another central pixel are examined (step 464) and the process returns to step 424. If, on the other hand, all of the image data for the given input image has been processed, then the image data of the given input image is prepared for output.

[0041] Referring to Figure 16, in one example of output, namely marking, the image data is transmitted to the printer 20, the printer 20 including a component 456 referred to as a pulse width position modulator ("PWPM"). As is known, the PWPM serves to control the operation of a raster output scanner ("ROS") as a function of digital input provided thereto. In the illustrated embodiment of Figure 16, the PWPM is responsive to the representative bits of a given pixel and, where appropriate, a positional signal so that three output pixels are reproduced by the ROS on the basis of the two or three bits provided to the PWPM. In one example, as shown in Figure 16, when the input data is a 01 and the positional signal is 1, the output includes two white pixels and one black pixel with the black pixel being left justified.

[0042] Numerous features of the above-disclosed embodiment will be appreciated by those skilled in the art:

[0043] First, the present technique includes an encoding approach which permits m out of every n bits to be discarded from image data of an input image where the m bits represent "positional" bits and n - m bits correspond with 2^{n-m} intensities. This discarding of bits results in a decrease of storage demand. In one example a storage saving of up to 33% is achieved. In some cases, such as the ones in which a pixel is all white or all black, the discarded bit will not be missed. That is, in some instances, it is possible to describe, completely, the output states of n bits with just n - m bits. In any event, "lost" information provided by the discarded bits is, where necessary, reconstructed, so there is little or no loss in image output quality.

[0044] Reconstruction is preferably accomplished by examining each pixel in an image and assigning a positional signal, when appropriate. Such reconstruction is believed to be necessary when the position of one or two black pixels, disposed in a group of three pixels cannot be positioned or justified on the basis of two bits worth of image information. Due to the assignment of the positional signals, virtually all of the information, related to the input image, can be recaptured for output.

[0045] Second, each positional signal is assigned with a high degree of accuracy. In one example, when a pixel being examined is framed by two pixels of the same intensity, e.g. white pixels, corresponding pixels from adjacent scanlines are analyzed to optimize eventual justification of one or more black pixels. Additionally, the examined pixels of the multiple scanlines can be analyzed in parallel so that the best suited positional signal can be obtained within a relatively short time interval.

[0046] Finally, relatively little hardware and software are required to implement the present technique. More particularly, each time a bit is discarded, an efficient encoding scheme is employed to compensate for much of the apparent loss in information. Moreover, pursuant to output of the encoded data, use of a simple, yet intuitive algorithm provides for the assignment of the positional signals. This algorithm is implemented with a minimum amount of hardware and, in one example, a suitable implementation can be achieved with relatively few logical components and a single look-up table.

Claims

1. A method of processing an input image with a printing system (10) having an electronic volatile memory (74), said input image being represented by image data, in the form of a data stream, comprising a plurality of successive bits grouped into first bit sets (411A, 411B, 411C)
each set comprising n bits, comprising the steps of:

encoding (402) said first bit sets into second bit sets (00, 01, 10, 11), each of the second bit sets having less bits (n-m) than each of the first bit sets, m being the number of discarded bits in each bit set as a result of said encoding;

storing (406) the encoded bit stream in the electronic volatile memory (74) with memory space being saved as a result of reducing a size of each of the first bit sets;

analyzing the stored encoded bit stream by defining a center second bit set disposed between a left second bit set and a right second bit set, respectively, for generating a corresponding signal assigned to said center second bit set and determined by comparing the intensities of said left second bit set and said right second bit set;

reconstructing the stored encoded bit stream, by converting the second bit sets to third bit

sets, each of said third bit sets again having n bits, the bits of said center bit set being arranged on the basis of said signal such that the bits representing black colour of said center bit set are associated to that one of said left or right neighbouring bit sets possessing the greater intensity; and

outputting an image representation of the reconstructed bit stream.

2. The method of claim 1, in which each first and second bit set corresponds with a pixel and the pixels are disposed in a plurality of scanlines, wherein said analyzing step is performed on each scanline.

3. The method of claim 2, further comprising the step of providing a look-up table (415), in a second electronic memory (434), the look-up table including a plurality of intensity pairs, each pair being mapped to one of said signals, respectively, and wherein: said analyzing step includes matching the respective intensities of the pixels left and right to a center pixel with one of the intensity pairs in the look-up table to obtain said corresponding signal.

4. The method of claim 3, in which, where the intensity of the left pixel is the same as that one of the right pixel, said analyzing step analyzes:

at least one neighbouring scanline (428) with a fourth pixel disposed between a fifth pixel and a sixth pixel at a position corresponding to the position of said center, left and right pixels respectively and examining the respective intensities of the fifth and sixth pixels; and

determining said signal of the center pixel in accordance with the signals obtained by analyzing the at least one neighbouring scanline.

5. The method of one of claims 1 to 4, wherein said outputting step comprises printing the image, on a substrate, with a print engine (20).

6. The method of one of claims 1 to 5, wherein said encoding step includes encoding the bit stream with an image processing device (22).

7. An apparatus for processing an input image represented by image data in the form of a data stream comprising a plurality of successive bits grouped into first bit sets (411A, 411B, 411C), each bit set comprising n bits, comprising:

a device for encoding (62) said first bit sets into second bit sets (00, 01, 10, 11), each of the second bit sets having less bits (n-m) than each of the first bit sets, m being the number of discarded bits in each bit set as a result of said encoding;

an electronic volatile memory (74) for storing (406) the encoded bit stream in the electronic volatile memory (74) with memory space being saved as a result of reducing a size of each of the first bit sets;

a bit stream analyzer (415, 432, 440; 434) for analyzing the stored encoded bit stream by defining a center second bit set disposed between a left second bit set and a right second bit set, respectively for generating a corresponding signal assigned to said center second bit set and determined by comparing the intensities of said left second bit set and said right second bit set;

a reconstruction circuit (64; 20) for reconstructing the stored encoded bit stream by converting the second bit sets to third bit sets, each of said third bit sets again having n bits, the bits of said center bit set being arranged on the basis of said signal, such that the bits representing black color of said center bit set are associated to that one of said left or right neighbouring bit sets possessing the greater intensity; and

an output device (20; 51, 28) for outputting an image representation of the reconstructed bit stream.

8. The image processing apparatus of claim 7, in which each first and second bit set corresponds with a pixel and the pixels are disposed in a plurality of scanlines (411, 428, 438).

9. The image processing apparatus of claim 8, in which said bitstream analyzer (415, 440; 434) includes a look-up table (LUT, 415), in a second electronic memory (432), the look-up table including a plurality of intensity pairs, each pair being mapped to one of said signals, respectively, and wherein the respective intensities of the pixels left and right to a center pixel are matched in the bitstream analyzer with one of the intensity pairs in the look-up table to obtain the corresponding signal.

10. The image processing apparatus of claim 9, in which, where the intensity of the left pixel is the same as that one of the right pixel, said bitstream analyzer analyzes at least one neighbouring scanline (428) with a fourth pixel disposed between a fifth pixel and a sixth pixel at a position corresponding to the position of said center, left and right pixels respectively; examines the respective intensities of

the fifth and sixth pixels, and determines said signal of the center pixel in accordance with the signals obtained by analyzing said at least one neighbouring scanline.

Patentansprüche

1. Verfahren zum Verarbeiten eines Eingangs-Bilds mit einem Drucksystem (10), das einen elektronischen, flüchtigen Speicher (74) besitzt, wobei das Eingangs-Bild durch Bild-Daten, in der Form einer Datenfolge, dargestellt ist, aufweisend eine Vielzahl von aufeinanderfolgenden Bits, die in erste Bit-Sätze (411A, 411B, 411C) gruppiert sind, wobei jeder Satz n Bits aufweist, mit den Schritten:

   Codieren (402) der ersten Bit-Sätze in zweite Bit-Sätze (00, 01, 10, 11), wobei jeder der zweiten Bit-Sätze weniger Bits (n-m) als jeder der ersten Bit-Sätze besitzt, wobei m die Zahl von ausgesonderten Bits in jedem Bit-Satz als eine Folge des Codierens ist;
   Speichern (406) der codierten Bit-Folge in dem elektronischen, flüchtigen Speicher (74), wobei Speicherraum als Folge eines Reduzierens einer Größe jedes der ersten Bit-Sätze eingespart wird;
   Analysieren der gespeicherten, codierten Bit-Folge durch Definieren eines zentralen, zweiten Bit-Satzes, angeordnet zwischen einem linken, zweiten Bit-Satz und einem rechten, zweiten Bit-Satz jeweils, zum Erzeugen eines entsprechenden Signals, das zu dem mittleren, zweiten Bit-Satz zugeordnet ist und durch Vergleichen der Intensitäten des linken, zweiten Bit-Satzes und des rechten, zweiten Bit-Satzes bestimmt ist;
   Rekonstruieren der gespeicherten, codierten Bit-Folge durch Wandeln der zweiten Bit-Sätze zu dritten Bit-Sätzen, wobei jeder der dritten Bit-Sätze wiederum n Bits besitzt, wobei die Bits des mittleren Bit-Satzes auf der Basis des Signals so angeordnet werden, daß die Bits, die eine schwarze Farbe des mittleren Bit-Satzes darstellen, zu dem einen des linken oder rechten, benachbarten Bit-Satzes zugeordnet werden, der die größere Intensität besitzt; und
   Ausgeben einer Bild-Darstellung der rekonstruierten Bit-Folge.

2. Verfahren nach Anspruch 1, wobei jeder erste und zweite Bit-Satz einem Pixel entspricht und die Pixel in einer Mehrzahl von Abtastlinien angeordnet sind, wobei der analysierende Schritt in Bezug auf jede Abtastlinie durchgeführt wird.

3. Verfahren nach Anspruch 2, das weiterhin den Schritt eines Vorsehens einer Durchsichtstabelle (415), in einem zweiten, elektronischen Speicher (434), aufweist, wobei die Durchsichtstabelle eine Vielzahl von Intensitäts-Paaren umfaßt, wobei jedes Paar zu einem der Signale jeweils aufgelistet wird, und wobei:

   der analysierende Schritt ein Anpassen der jeweiligen Intensitäten der Pixel links und rechts zu einem mittleren Pixel mit einem der Intensitäts-Paare in der Durchsichtstabelle, um das entsprechende Signal zu erhalten, umfaßt.

4. Verfahren nach Anspruch 3, wobei dort, wo die Intensität des linken Pixels dieselbe wie die eine des rechten Pixels ist, der analysierende Schritt analysiert

   mindestens eine benachbarte Abtastlinie (428) mit einem vierten Pixel, angeordnet zwischen einem fünften Pixel und einem sechsten Pixel an einer Position entsprechend zu der Position des mittleren, linken und rechten Pixels jeweils, und wobei die jeweiligen Intensitäten des fünften und sechsten Pixels geprüft werden; und
   wobei das Signal des mittleren Pixels entsprechend den Signalen, die durch Analysieren der mindestens einen benachbarten Abtastlinie erhalten sind, bestimmt wird.

5. Verfahren nach einem der Ansprüche 1 bis 4, wobei der Ausgabe-Schritt ein Drukken des Bilds, auf einem Substrat, mit einer Druckmaschine (20) aufweist.

6. Verfahren nach einem der Ansprüche 1 bis 5, wobei der Codier-Schritt ein Codieren der Bit-Folge mit einer Bildverarbeitungs-Vorrichtung (22) umfaßt.

7. Vorrichtung zum Verarbeiten eines Eingangs-Bilds, das durch Bild-Daten, in der Form einer Datenfolge, dargestellt ist, die eine Vielzahl von aufeinanderfolgenden Bits aufweist, die in erste Bit-Sätze (411A, 411B, 411C) gruppiert sind, wobei jeder Bit-Satz n Bits aufweist, mit:

   einer Vorrichtung zum Codieren (62) der ersten Bit-Sätze in zweite Bit-Sätze (00, 01, 10, 11), wobei jeder der zweiten Bit-Sätze weniger Bits (n-m) als jeder der ersten Bit-Sätze besitzt, wobei m die Zahl von ausgesonderten Bits in jedem Bit-Satz als Folge des Codierens ist;
   einem elektronischen, flüchtigen Speicher (74) zum Speichern (406) der codierten Bit-Folge in dem elektronischen, flüchtigen Speicher (74), wobei Speicherraum als eine Folge eines Reduzierens einer Größe jeder der ersten Bit-Sätze eingespart wird;

einem Bit-Folge-Analysierer (415, 432, 440; 434) zum Analysieren der gespeicherten, codierten Bit-Folge durch Definieren eines mittleren, zweiten Bit-Satzes, angeordnet zwischen einem linken, zweiten Bit-Satz und einem rechten, zweiten Bit-Satz jeweils, zum Erzeugen eines entsprechenden Signals, das dem mittleren, zweiten Bit-Satz zugeordnet ist und durch Vergleichen der Intensitäten des linken, zweiten Bit-Satzes und des rechten, zweiten Bit-Satzes, bestimmt ist;
einer Rekonstruktions-Schaltung (64; 20) zum Rekonstruieren der gespeicherten, codierten Bit-Folge durch Wandeln der zweiten Bit-Sätze in dritte Bit-Sätze, wobei jeder der dritten Bit-Sätze wiederum n Bits besitzt, wobei die Bits des mittleren Bit-Satzes auf der Basis des Signals angeordnet werden, so daß die Bits, die eine schwarze Farbe des mittleren Bit-Satzes darstellen, zu demjenigen einen des linken oder rechten, benachbarten Bit-Satzes, der die größere Intensität besitzt, zugeordnet sind; und
einer Ausgabe-Vorrichtung (20; 51, 28) zum Ausgeben einer Bild-Darstellung der rekonstruierten Bit-Folge.

8. Bildverarbeitungs-Vorrichtung nach Anspruch 7, wobei jeder erste und zweite Bit-Satz einem Pixel entspricht und die Pixel in einer Vielzahl von Abtastlinien (411, 428, 438) angeordnet sind.

9. Bildverarbeitungs-Vorrichtung nach Anspruch 8, wobei der Bit-Folge-Analysierer (415, 440; 434) eine Durchsichtstabelle (LUT; 415), in einem zweiten, elektronischen Speicher (492), umfaßt, wobei die Durchsichtstabelle eine Vielzahl von Intensitäts-Paaren umfaßt, wobei jedes Paar zu einem der Signale jeweils aufgelistet ist, und wobei die jeweiligen Intensitäten der Pixel links und rechts zu einem mittleren Pixel in dem Bit-Folge-Analysierer zu einem der Intensitäts-Paare in der Durchsichtstabelle angepaßt sind, um das entsprechende Signal zu erhalten.

10. Bildverarbeitungs-Vorrichtung nach Anspruch 9, wobei dort, wo die Intensität des linken Pixels dieselbe wie diejenige eine des rechten Pixels ist, der Bit-Folge-Analysierer mindestens eine benachbarte Abtastlinie (428) analysiert, mit einem vierten Pixel, das zwischen einem fünften Pixel und einem sechsten Pixel an einer Position entsprechend zu der Position des mittleren, linken und rechten Pixels jeweils angeordnet ist; die jeweiligen Intensitäten des fünften und sechsten Pixels prüft und das Signal des mittleren Pixels entsprechend den Signalen, die durch Analysieren der mindestens einen benachbarten Abtastlinie erhalten sind, bestimmt.

Revendications

1. Procédé de traitement d'une image d'entrée avec un système d'impression (10) comportant une mémoire électronique volatile (74), ladite image d'entrée étant représentée par des données d'image, sous forme d'un flux de données, comprenant une pluralité de bits successifs regroupés en des premiers ensembles de bits (411A, 411B, 411C),
chaque ensemble comprenant n bits, comprenant les étapes consistant à :

coder (402) lesdits premiers ensembles de bits en des seconds ensembles de bits (00, 01, 10, 11), chacun des seconds ensembles de bits présentant moins de bits (n - m) que chacun des premiers ensembles de bits, m étant le nombre des bits rejetés dans chaque ensemble de bits en tant que résultat dudit codage,
mémoriser (406) le flux de bits codé dans la mémoire électronique volatile (74) avec un espace de mémoire économisé en tant que résultat de la réduction de la taille de chacun des premiers ensembles de bits,
analyser le flux de bits codé mémorisé en définissant un second ensemble de bits central disposé entre un second ensemble de bits de gauche et un second ensemble de bits de droite, respectivement, afin de générer un signal correspondant affecté audit second ensemble de bits central et déterminé en comparant les intensités dudit second ensemble de bits de gauche et dudit second ensemble de bits de droite,
reconstituer le flux de bits codé mémorisé en convertissant les seconds ensembles de bits en troisièmes ensembles de bits, chacun desdits troisièmes ensembles de bits comportant à nouveau n bits, les bits dudit ensemble de bits central étant agencés sur la base dudit signal de sorte que les bits représentant une couleur noire dudit bit central sont associés à celui desdits ensembles de bits voisins de gauche ou de droite qui possèdent l'intensité la plus grande, et
fournir en sortie une représentation en image du flux de bits reconstitué.

2. Procédé selon la revendication 1, dans lequel chacun des premier et second ensembles de bits correspond à un pixel et les pixels sont disposés dans une pluralité de lignes de balayage, dans lequel ladite étape d'analyse est exécutée sur chaque ligne de balayage.

3. Procédé selon la revendication 2, comprenant en outre l'étape consistant à fournir une table de consultation (415), dans une seconde mémoire électronique (434), la table de consultation comprenant

une pluralité de paires d'intensités, chaque paire étant mappée sur l'un desdits signaux, respectivement, et dans lequel :

ladite étape d'analyse comprend la mise en correspondance des intensités respectives des pixels à gauche et à droite d'un pixel central avec l'une des paires d'intensités dans la table de consultation afin d'obtenir ledit signal correspondant.

4. Procédé selon la revendication 3, dans lequel, lorsque l'intensité du pixel de gauche est la même que celle du pixel de droite, ladite étape d'analyse analyse :

au moins une ligne de balayage voisine (428) avec un quatrième pixel disposé entre un cinquième pixel et un sixième pixel à une position correspondant à la position desdits pixels du centre, de gauche et de droite, respectivement et en examinant les intensités respectives des cinquième et sixième pixels, et
en déterminant ledit signal du pixel central conformément aux signaux obtenus en analysant la au moins une ligne de balayage voisine.

5. Procédé selon l'une des revendications 1 à 4, dans lequel ladite étape de sortie comprend l'impression de l'image, sur un substrat, avec un moteur d'impression (20).

6. Procédé selon l'une des revendications 1 à 5, dans lequel ladite étape de codage comprend le codage du flux de bits avec un dispositif de traitement d'image (22).

7. Dispositif destiné à traiter une image d'entrée représentée par des données d'image sous forme d'un flux de données comprenant une pluralité de bits successifs regroupés en des premiers ensembles de bits (411A, 411B, 411C), chaque ensemble de bits comprenant n bits, comprenant :

un dispositif destiné à coder (62) lesdits premiers ensembles de bits en des seconds ensembles de bits (00, 01, 10, 11), chacun des seconds ensembles de bits comportant moins de bits (n - m) que chacun des premiers ensembles de bits, m étant le nombre des bits rejetés dans chaque ensemble de bits en tant que résultat dudit codage,
une mémoire électronique volatile (74) destinée à mémoriser (406) le flux de bits codé dans la mémoire électronique volatile (74), de l'espace de la mémoire étant économisé en tant que résultat de la réduction d'une taille de chacun des premiers ensembles de bits,
un analyseur de flux de bits (415, 432, 440 ; 434) destiné à analyser le flux de bits codé mémorisé en définissant un second ensemble de bits central disposé entre un second ensemble de bits de gauche et un second ensemble de bits de droite, respectivement afin de générer un signal correspondant affecté audit second ensemble de bits central et déterminé en comparant les intensités dudit second ensemble de bits de gauche et dudit second ensemble de bits de droite,
un circuit de reconstitution (64 ; 20) destiné à reconstituer le flux de bits codé mémorisé en convertissant les seconds ensembles de bits en des troisièmes ensembles de bits, chacun desdits troisièmes ensembles de bits comportant à nouveau n bits, les bits dudit ensemble de bits central étant agencés sur la base dudit signal, de sorte que les bits représentant une couleur noire dudit ensemble de bits central sont associés à celui des ensembles de bits voisins de gauche ou de droite possédant l'intensité la plus grande, et
un dispositif de sortie (20 ; 51, 28) destiné à fournir en sortie une représentation en image du flux de bits reconstitué.

8. Dispositif de traitement d'image selon la revendication 7, dans lequel chacun des premier et second ensembles de bits correspond à un pixel et les pixels sont disposés dans une pluralité de lignes de balayage (411, 428, 438).

9. Dispositif de traitement d'image selon la revendication 8, dans lequel ledit analyseur de flux de bits (415, 440 ; 434) comprend une table de consultation (LUT ; 415), dans une seconde mémoire électronique (432), la table de consultation comprenant une pluralité de paires d'intensités, chaque paire étant mappée sur l'un desdits signaux, respectivement, et dans lequel les intensités respectives des pixels à gauche et à droite d'un pixel central sont mises en correspondance dans l'analyseur de flux de bits avec l'une des paires d'intensités de la table de consultation afin d'obtenir le signal correspondant.

10. Dispositif de traitement d'image selon la revendication 9, dans lequel, lorsque l'intensité du pixel de gauche est la même que celle du pixel de droite, ledit analyseur de flux de bits analyse au moins une ligne de balayage voisine (428) avec un quatrième pixel disposé entre un cinquième pixel et un sixième pixel à une position correspondant à la position desdits pixels du centre, de gauche et de droite, respectivement, examine les intensités respectives des cinquième et sixième pixels, et détermine ledit signal du pixel central conformément aux signaux obtenus en analysant ladite au moins une ligne de balayage voisine.

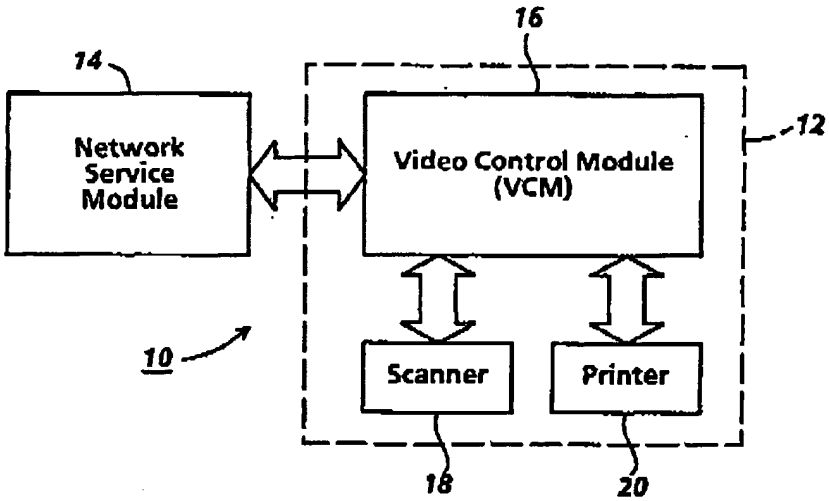

FIG. 1

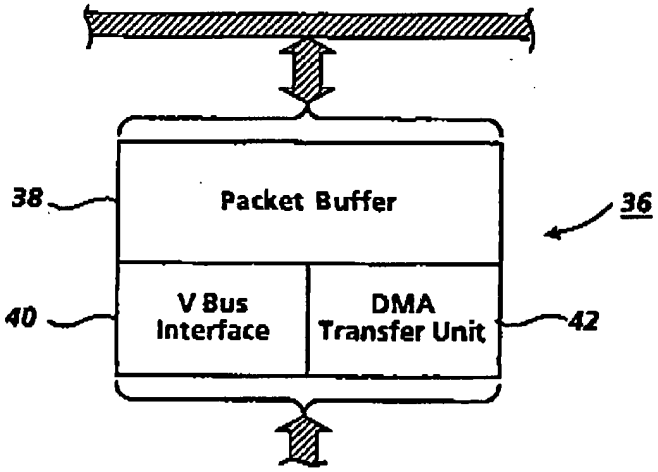

FIG. 3

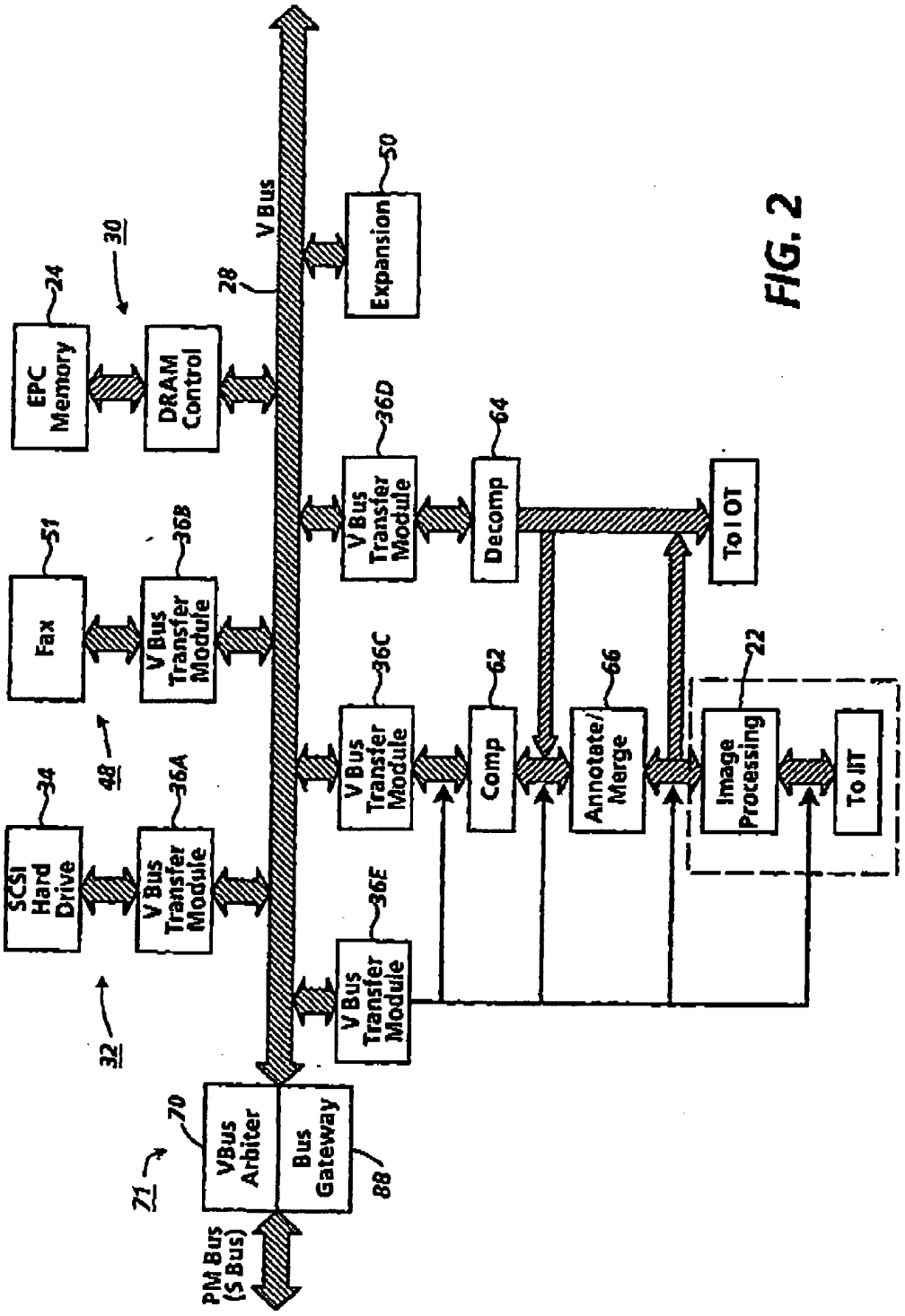

FIG. 2

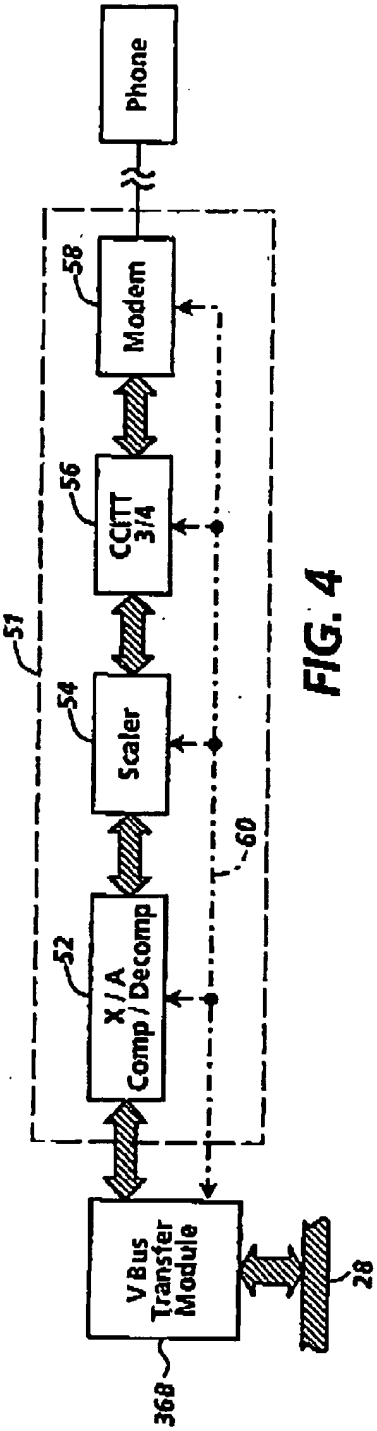

FIG. 4

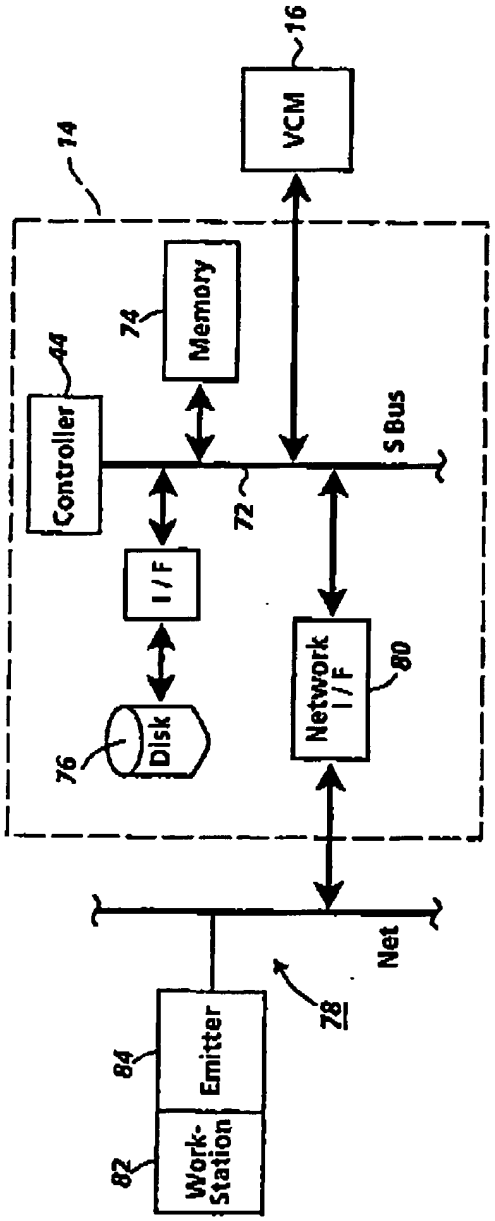

FIG. 5

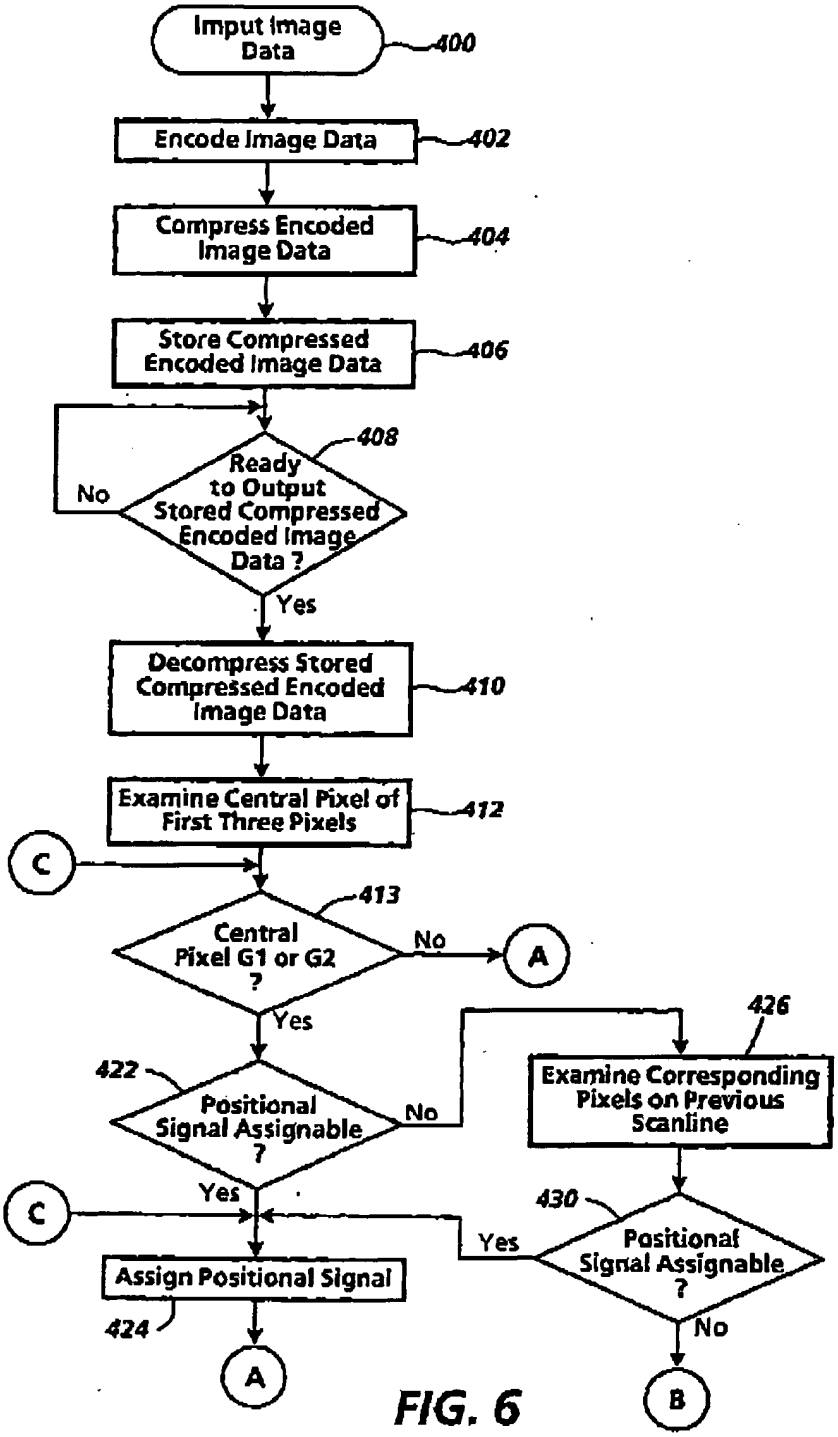

FIG. 6

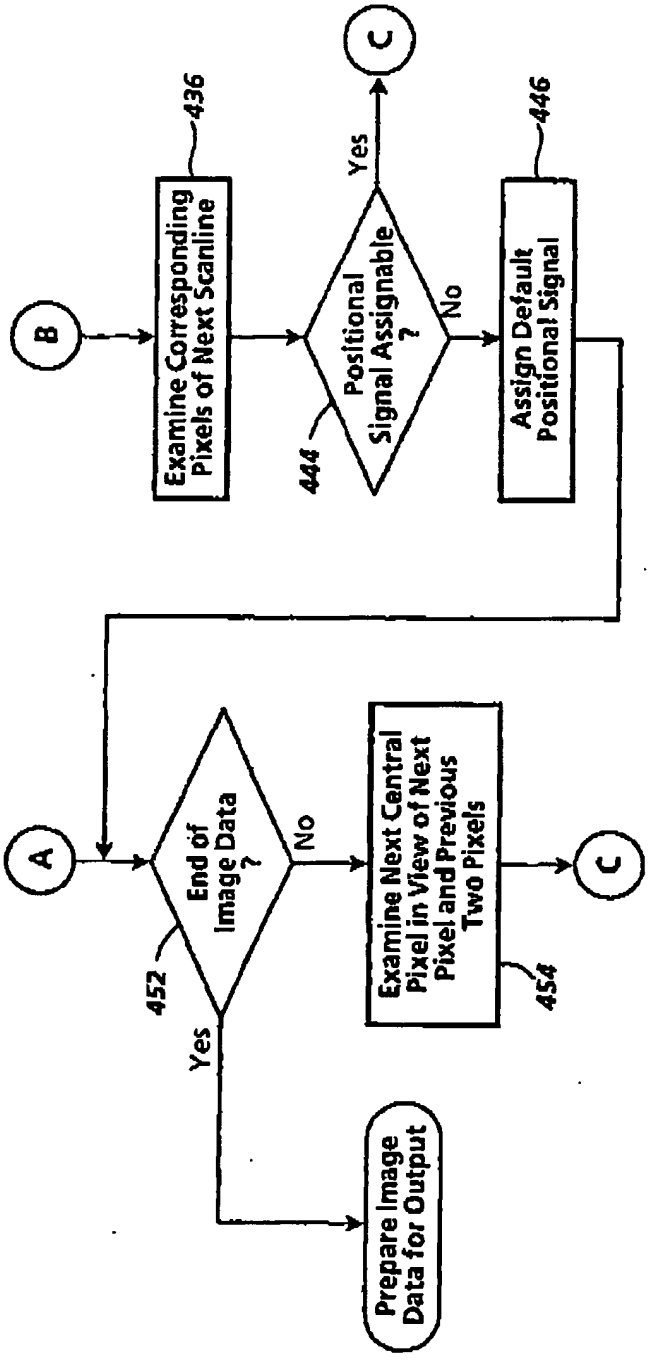
A
B
C
End of Image Data ?
452
No
Yes
Examine Next Central Pixel in View of Next Pixel and Previous Two Pixels
454
C
Prepare Image Data for Output
Examine Corresponding Pixels of Next Scanline
436
Positional Signal Assignable ?
444
Yes
No
C
Assign Default Positional Signal
446

FIG. 7

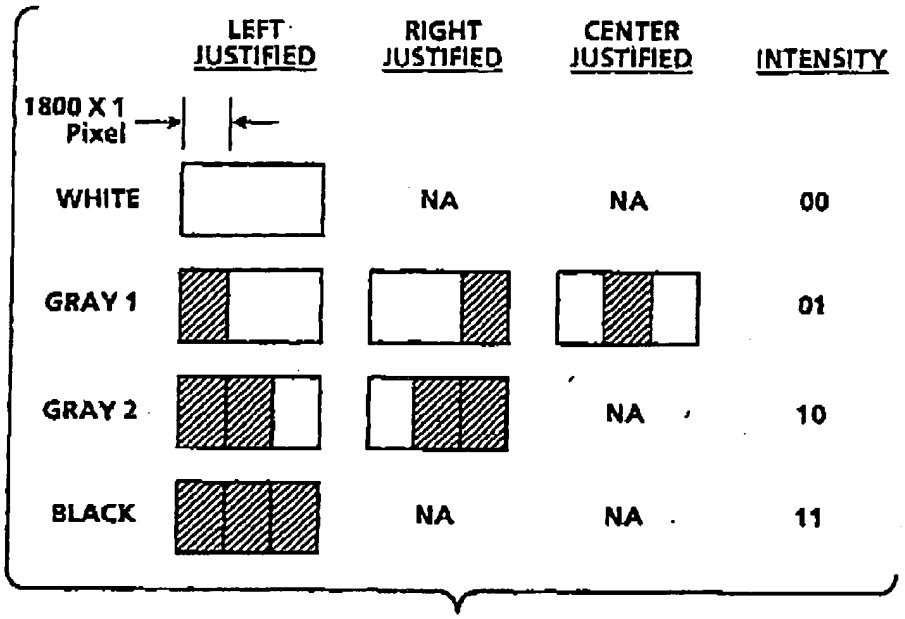

FIG. 8

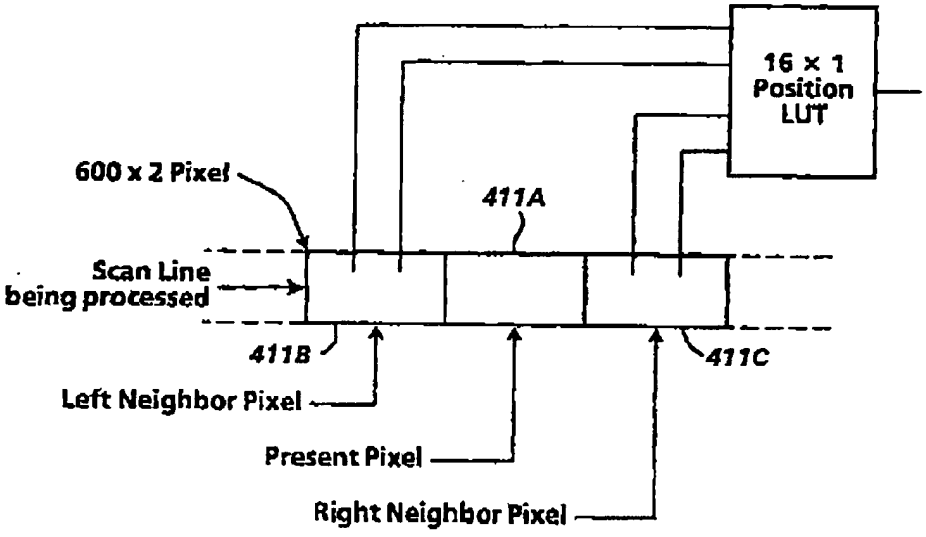

FIG. 9

Left Neighbor Pixel	Present Pixel	Right Neighbor Pixel	POSITION	VALUE
W		W	L	1
W		G1	R	0
W		G2	R	0
W		B	R	0
G1		W	L	1
G1		G1	R	0
G1		G2	R	0
G1		B	R	0
G2		W	L	1
G2		G1	L	1
G2		G2	L	1
G2		B	R	0
B		W	L	1
B		G1	L	1
B		G2	L	1
B		B	R	0

415

FIG. 10

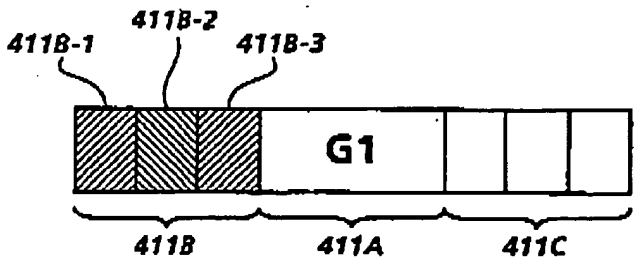

FIG. 11A

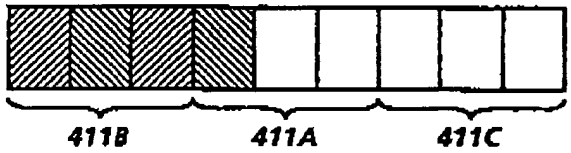

FIG. 11B

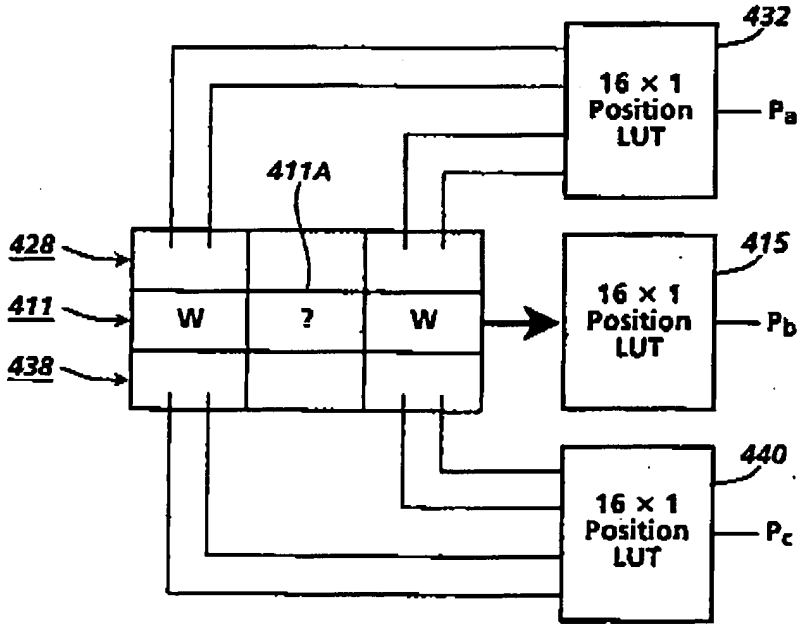

FIG. 12

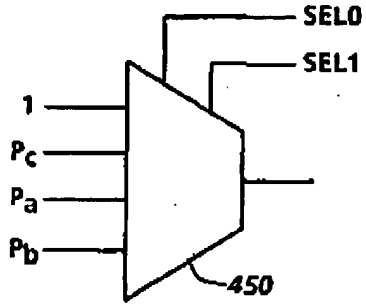

FIG. 13

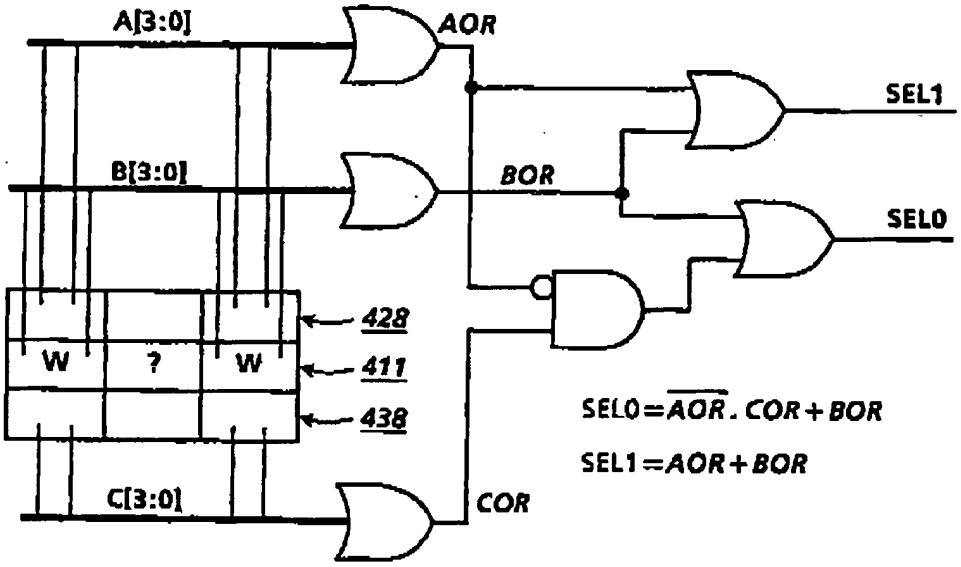

FIG. 14

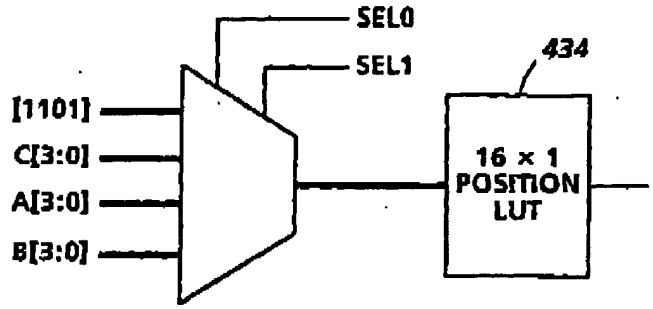

FIG. 15

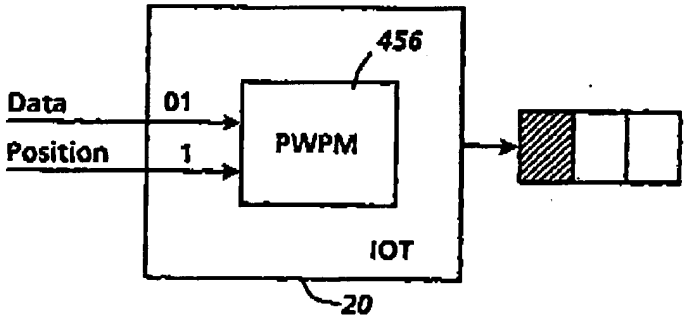

FIG. 16